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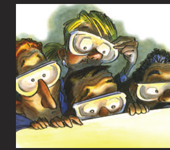

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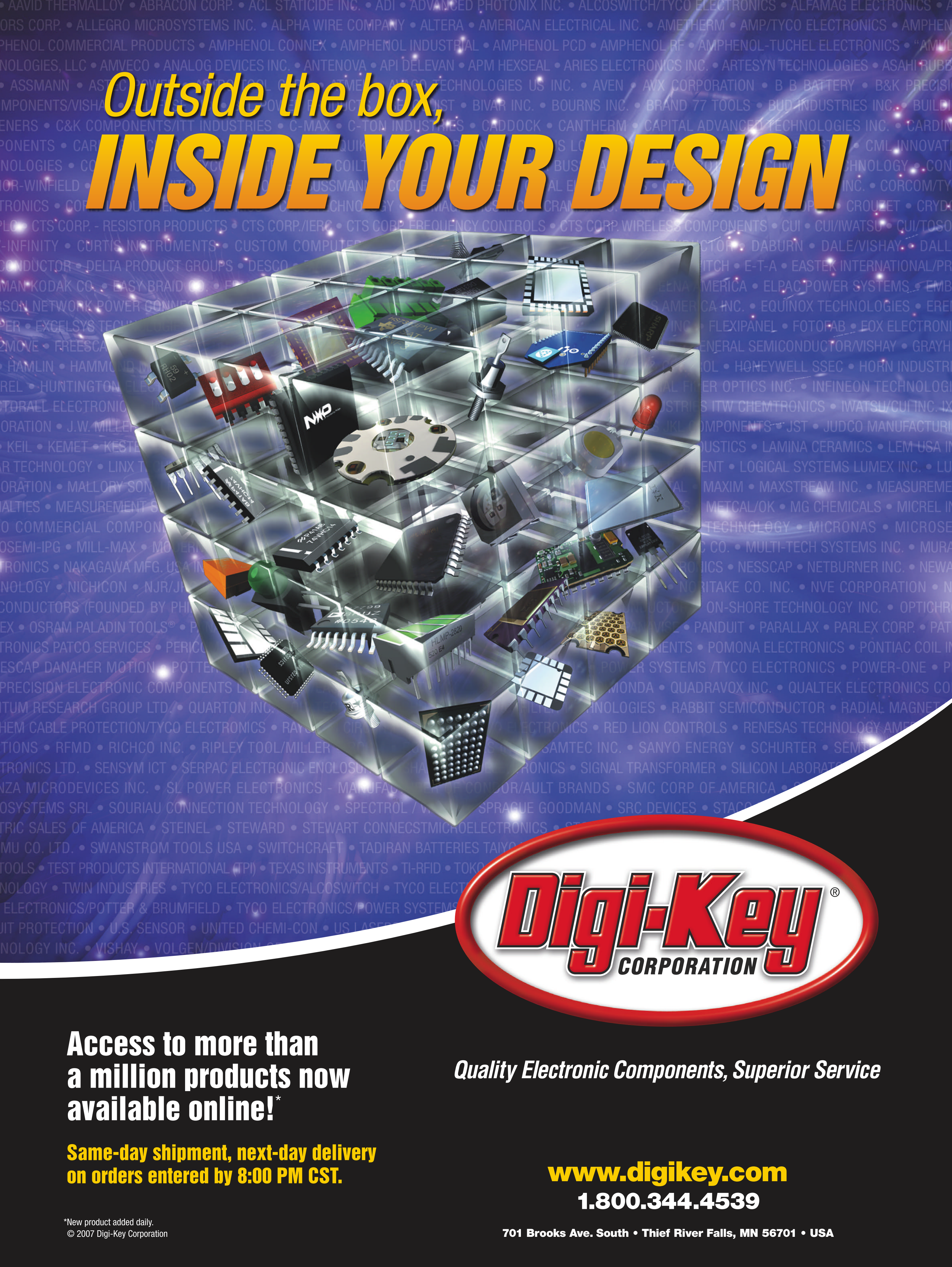
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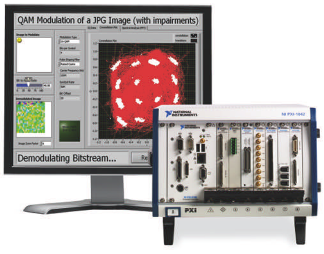

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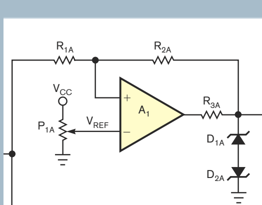


Connect...
to PCI Express, Gigabit Ethernet
& Serial RapidIO

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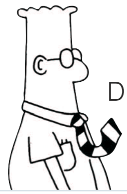

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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Enterprise applications go embedded
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LSI acquires content-inspection experts Tarari
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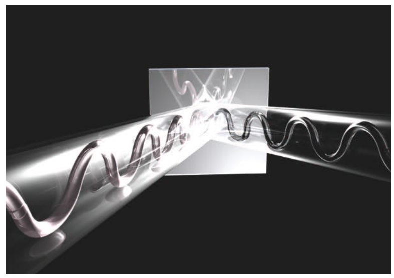

READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

TDR: taking the pulse of signal integrity
Time-domain reflectometry will help you design and troubleshoot cables, connectors, fast PCB traces, and high-speed packages. Both analog and digital engineers need to understand and use TDR techniques.
→www.edn.com/article/CA6470825

No Moore's Law for batteries: Improvements come in dribs and drabs
→www.edn.com/070927toc1

Inside Apple's iPhone: More than just a dial tone
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Question your assumptions: a cautionary Windows Vista case study
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Printed electronics: ink on the brink
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White-LED driver operates down to 1.2V supply voltage
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Recognizing gestures: interface design beyond point and click
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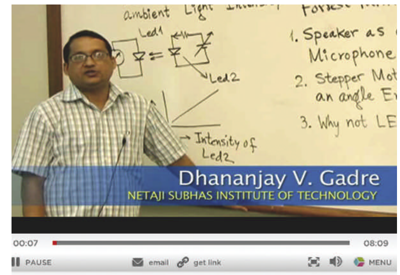
Single-supply amplifier outputs don't swing rail to rail
→www.edn.com/article/CA6470824



VIDEO DESIGN IDEAS

LED senses, displays light intensity
Dhananjay V Gadre of India's Netaji Subhas Institute of Technology explains how an LED can double as a photosensor and a visual indicator of ambient-light intensity.
→www.edn.com/article/CA6475381

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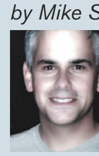
FROM *EDN*'s BLOGS

Who is the EDA leader in SystemVerilog simulation?
From Between The Lines, by Mike Santarini



"Collaboration," "cooperation," "open," and "interoperability" are words that users and the EDA press embrace. But behind just about every "open-standards" proposal in EDA is an ulterior motive—and, more times than not, a new "open effort" is simply two or more smaller players trying to gang up on and gain share from a dominant player in an EDA submarket.
→www.edn.com/070927toc3

Will 4G wireless ever really happen?
From Practical Chip Design, by Ron Wilson

Real 4G requires about a half-order of magnitude increase in the number of bits per second and per hertz of channel bandwidth compared with existing services. This, in turn, requires better noise floors, channel equalization, linearity, data recovery, and compression. None of those things will come easily.
→www.edn.com/070927toc4

BY MAURY WRIGHT, EDITORIAL DIRECTOR

Reach is key to broadband-based innovation

Watch the popular press, and you will constantly hear about how far behind the United States is when it comes to broadband deployment and the more recent move to 100-Mbps and faster data rates. The follow-on assertion typically suggests that the lack of such broadband access will cripple innovation in the United States. But such assertions seem always to pinpoint speed/bandwidth as the issue. Actually, we have a more critical access problem with much of our rural or semirural population.

An article I just read, "Japan's bullet-train ride to Internet future," prompted me to write this column. The article originated at *The Washington Post*, although I read it in the *San Diego Union Tribune* (www.signonsandiego.com/uniontrib/20070904/news_1b4japannet.html).

The article made the typical point that Japan and other places such as Korea and Europe have far superior broadband performance to that of the United States. It also offered some interesting examples of broadband-enabled innovation. For instance, it described a remote telemedicine application whereby a pathologist could directly connect to remote microscopes in real time to examine tissue. Presumably, patients that live far from a fully equipped medical facility could still receive top-notch care—assuming the remote facility had the requisite microscope and broadband link. I'm sure there is some validity to that example.

Still, I felt that the article really glossed over the issues that we face in North America relative to a country such as Japan. Moreover, the article was too quick to suggest a government-subsidized fiber build-out such as the one that has taken place in Japan.

The real problem in North America isn't data rate. Sure, it would be great if we could receive any video that we desire in high-definition quality in real time over the Internet. But for the most part, people who have broadband are pretty happy with the performance. Indeed, the always-on nature of the service remains more attractive than the data rate. Try a session of Xbox Live multiplayer gaming, and you will discover that a cable modem or a DSL link handles such interactive applications very well—including the inherent VOIP (voice-over-Internet Protocol) conferencelike call that allows players to talk during a session.

Our problem really centers on the fact that too many people just can't get broadband, even today. Two of our *EDN* technical editors are limited to satellite Internet service, and both live fairly near well-populated areas. The satellite service is better than dial-up service, but it doesn't run our corporate VPN (virtual private network).

The broadband situation is somewhat analogous to the home-wireless-network situation. I've long argued that range in 802.11 wireless LANs is more important than data rate. We also need to get a truly functional broadband link to those network-enabled homes. The United States is much larger than Japan, with a geographically diverse population and a bent toward single-family homes. And you don't have to be far from the heart of Silicon Valley to find yourself without broadband coverage.

With any luck, WiMax technology will close the broadband gap in semirural settings. Where I live in San Diego, a service provider, Skyriver Communications (www.skyriver.net), is advertising heavily on local radio. The company's price is about double that of my cable-modem-service price but still reasonable. I hope that we at *EDN* will have some hands-on testing of Skyriver or another WiMax service in the near future.

I'm also encouraged that Sprint (www.sprint.com) and Clearwire (www.clearwire.com) have agreed to partner on WiMax deployment. The companies have been the largest service providers to publicly support WiMax and start a broad network build-out. For background on WiMax and these companies, see www.edn.com/article/CA6426878. In June, Sprint and Clearwire agreed to build interoperable networks and to allow roaming between the two networks.

As much as I like the idea of fiber to the home, and I've written extensively on the subject, I'd hope we first figure out how to get a functional broadband link to everyone that wants one. Perhaps WiMax will deliver those links in the coming year.**EDN**

Contact me at mgwright@edn.com.

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Go to www.edn.com/070927ed and click on Feedback Loop to post a comment on this column.

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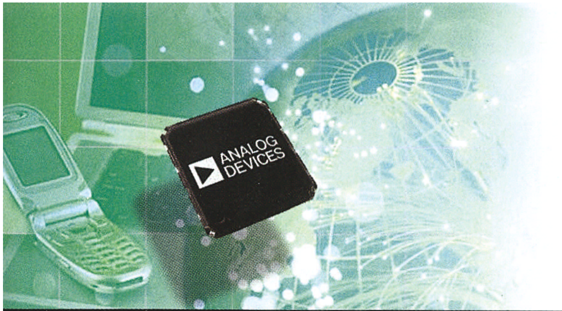

AMPLIFIER ICs

Volume 7, Issue 9

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Dual Difference Amplifiers Offer Higher System Performance and Channel Density at an Attractive Price

The AD8270 is a dual-channel, pin-programmable difference amplifier with internal gain setting resistors that offer unmatched dc precision with ac bandwidth specifications. The device combines 10 MHz of bandwidth and a 30 V/μs slew rate, making it ideally suited for advanced applications such as high speed industrial control measurement and multichannel systems where high bandwidth and SNR are required.

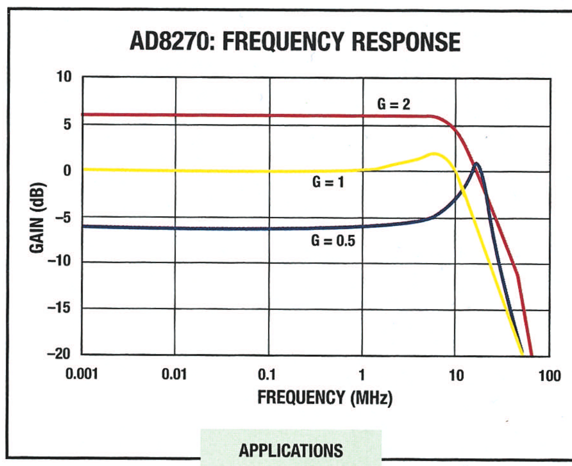
With no external components, the AD8270 can be configured as a high performance difference amplifier (G = 0.5, 1, or 2), inverting amplifier (G = 0.5, 1, or 2), or noninverting amplifier (G = 1.5, 2, or 3). It is offered in a 4 mm × 4 mm, 16-lead LFCSP, supporting double the channel density at a lower cost per channel vs. competitive solutions, with no compromise in performance.

A standard pinout 14-lead SOIC (G = 0.5 or 2) version of this device, the AD8273, is also available.

Both the AD8270 and AD8273 operate on single- and dual-supplies and only require 2.5 mA maximum supply current per amplifier. Each device is specified over the industrial temperature range of −40°C to +85°C and both are fully RoHS compliant.

The AD8270 is tailored to operate with the AD7621, AD7671, AD7674, AD7677, AD7678, AD7679, AD7685, AD7366, AD7367, AD7612, AD7951, AD7610, AD7631, AD7634, AD7946, and AD7947 PulSAR® ADCs, as well as the ADR431 and ADR435 voltage references.

- Bandwidth: >10 MHz
- Slew rate: 30 V/μs (AD8270), 25 V/μs (AD8273)
- Gain accuracy: 0.05%
- Gain drift: 10 ppm/°C
- Offset voltage: 400 μV
- CMRR: 86 dB



APPLICATIONS
- High performance audio
- Instrumentation amplifier building block
- Level translator
- Automatic test equipment
- Sin/cos encoders

AD8270 (16-lead LFCSP)	$1.99
AD8273 (14-lead SOIC)	$1.65

www.analog.com/V7Amplifiers2

ANALOG DEVICES

National Instruments' Popular Multisim SPICE Evaluation Software Goes Online to Simulate ADI Op Amps

Analog Devices and National Instruments' Electronics Workbench Group have teamed to introduce NI Multisim Analog Devices Edition—a free software download that enables designers to simulate circuit board designs and choose the optimal ADI components for their projects. Powered by industry-standard SPICE technology, NI Multisim Analog Devices Edition provides an intuitive environment for capturing and simulating analog circuits, including more than 400 ADI amplifier product models from which to choose and evaluate. By simulating your circuits to create virtual prototypes, you can detect errors early in the process and avoid costly and time consuming prototype reworking. You can also easily swap up to 26 components to evaluate your designs, ensuring you've chosen the right ADI amplifier for the job. This new download complements ADI's other tools to provide more options for the level of selection, evaluation, and circuit testing you need for your design.

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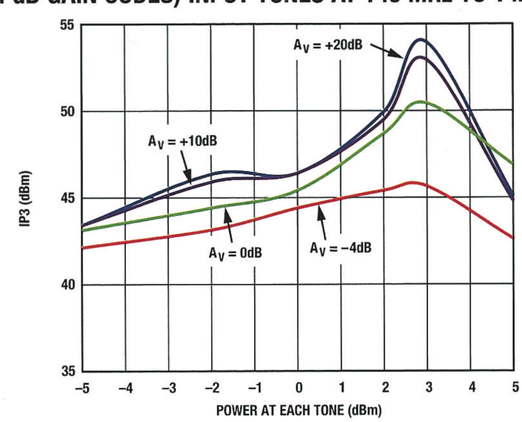
For more information, visit *www.analog.com/multisim*.

Single- and Dual-Channel Variable Gain Amplifiers (VGAs) Provide 1 dB Resolution for Digital IF Automatic Gain Control (AGC) Applications

The AD8375 (single) and AD8376 (dual) digitally controlled variable gain amplifiers provide precise 1 dB gain control across a 24 dB range. Both devices provide low distortion and high linearity with 50 dBm of output IP3, achieved through a proprietary distortion cancellation circuit. The AD8375 and AD8376 amplifiers are fully specified for IFs beyond 200 MHz. The devices consume 130 mA per channel and can be powered down to consume less than 5 mA from a single +5 V supply. They are available in 24-lead, 4 mm × 4 mm and 32-lead, 5 mm × 5 mm LFCSP packaging.

- Bandwidth: 690 MHz @ −3 dB
- Gain range: −4 dB to +20 dB
- Step size: 1 dB, ±0.2 dB
- Differential input: 150 Ω
- Differential output: open collector
- Noise figure: 8 dB @ maximum gain
- OIP3: 50 dBm @ 140 MHz

OUTPUT IP3 vs. OUTPUT POWER (+20 dB, +10 dB, 0 dB, −4 dB GAIN CODES) INPUT TONES AT 140 MHz TO 142 MHz



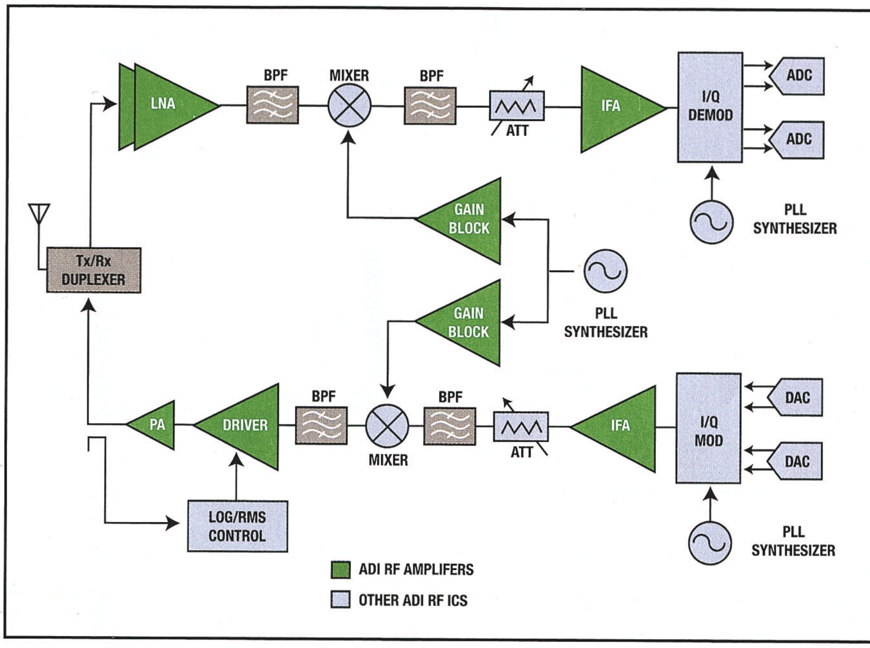
APPLICATIONS

- 3G and 4G wireless
- ATE
- Cable infrastructure
- Instrumentation

AD8375	$4.49
AD8376	$6.49

Fully Specified RF Amplifiers Across the Entire RF Signal Chain

Analog Devices' RF amplifiers are designed to support advanced RF radio architectures across a wide range of performance-driven applications, such as communications infrastructure equipment, medical equipment, marine radar, and RFID readers. Each RF amplifier family provides leading linearity performance, and is fully specified and characterized over temperature, supply voltage, and operating frequency to simplify the design-in process. Analog Devices RF amplifiers integrate internal active bias and internal matching, where appropriate, to minimize the external component count in low cost, small footprint, surface-mount packages.



Part Number	Frequency Range (MHz)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)	NF (dB)	Current (mA)	Specs @ (MHz)	Price ($U.S.)
Low Noise Amplifiers (LNA)								
ADL5521	400 to 4000	15.3	35.3	22.5	0.8	65	1950	2.15
ADL5523	400 to 4000	17.5	33.7	21.9	1.0	65	1950	2.15
Intermediate Frequency Amplifiers (IFA)								
ADL5530*	DC to 1000	16.8	37.0	21.8	3.0	110	190	1.56
ADL5531	20 to 500	20.3	40.9	20.7	2.7	101	190	2.25
ADL5532	20 to 500	16.1	39.1	19.7	3.0	95	70	2.25
ADL5533 (75 Ω)	30 to 1000	19.8	37.3	18.7	2.9	66	70	2.55
ADL5534 (Dual)	20 to 500	19.8	41.8	20.0	2.5	90	70	3.29
Gain Blocks								
AD8353*	1 to 2700	19.5	22.8	8.3	5.6	42	900	0.48
AD8354*	1 to 2700	19.5	19.3	4.8	4.4	25	900	0.48
ADL5541	50 to 6000	14.7	39.2	16.3	3.8	92	2000	1.65
ADL5542	50 to 6000	18.7	39.0	18.0	3.2	92	2000	1.65
Driver Amplifiers								
ADL5320	400 to 2700	13.7	42.0	25.6	4.2	104	2140	2.55
ADL5322	700 to 1000	19.9	45.3	27.9	5.0	320	900	3.48
ADL5323	1700 to 2400	19.5	43.5	28.0	5.0	320	2140	3.48
Part Number	**Frequency Range (MHz)**	**Gain (dB)**	**Linear P_{OUT} (dBm)**	**P1dB (dBm)**	**EVM (% rms)**	**Current (mA)**	**PAE (%)**	**Price ($U.S.)**
Power Amplifier								
ADL5570*	2300 to 2400	28	27.5	32	<3.0	10 to 300	20	5.00

*3 V bias is also supported.

Online seminar available on demand:
"Options and Solutions for RF System Design" at
www.analog.com/onlineseminars/RFSystems.

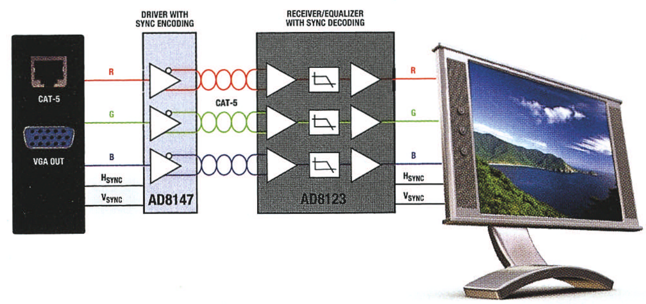
Triple High Speed Differential Receiver and Equalizer for Video Distribution Up to 300 Meters

The AD8123 is a triple high speed differential receiver and equalizer that compensates for the transmission losses of a variety of cables, including unshielded twisted pair (Cat-5) and video coaxial cables. The device restores the sharpness of UXGA video images up to 300 meters from the source. When used with AD8147 and AD8148 drivers, the video sync signals can be sent on the common mode and extracted by comparators included within the AD8123. The AD8123 is available in a 40-lead LFCSP package and operates over the extended temperature range of –40°C to +85°C.

- 55 dB gain at 100 MHz
- On-chip comparators for sync extraction
- Adjustable line equalization of UTP and coaxial cables up to 300 meters

Online seminar available on demand: "Broadband Video Distribution: Today's Challenges and Solutions" at *www.analog.com/onlinseminars/videodistribution*.

HD VIDEO OVER UTP



The AD8147 is a triple differential driver for wideband video.

APPLICATIONS

- HD video distribution over long distances
- RGB video over UTP cables
- Digital signage
- KVM
- Security video

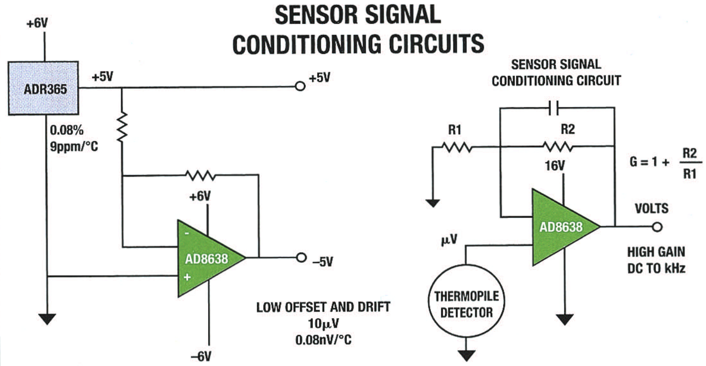
AD8123 $7.79

16 V Auto-Zero, Low Drift Offset Amplifier Minimizes Error Sources

The AD8638 is perfectly suited for sensor signal condition applications where error sources must be minimized. In the example below, the AD8638 is ideal as a thermopile amplifier where error contributions due to temperature, power supply, and voltage input range are difficult to compensate for without increasing design complexity and cost. The device is a single, wide bandwidth, auto-zero amplifier featuring rail-to-rail output swing while operating from 5 V to 16 V single supply or ±2.5 V to ±8 V dual supplies. The AD8638 is specified for the extended industrial temperature range of –40°C to +125°C and is available in 5-lead SOT-23 and 8-lead SOIC packaging.

- Offset voltage: 10 µV maximum
- Offset drift: 0.08 µV/°C
- CMRR: 140 dB
- PSRR: 140 dB
- Gain bandwidth: 1.5 MHz
- Input bias current: 100 pA
- Supply current: 1.4 mA/amp

SENSOR SIGNAL CONDITIONING CIRCUITS



The ADR365 is a low power, low noise voltage reference with sink/source capability, 5.0 V_{OUT}

APPLICATIONS

- Pressure and position sensors
- Strain gage amplifiers
- Medical instrumentation
- Thermocouple amplifiers
- Automotive sensors
- Precision references
- Precision current sources
- Electronic scales

AD8638 $0.88/100k $1.25/1k

Industry's First Dual ADC Drivers for High Speed 14-Bit and 16-Bit Converters

The ADA4937-2 and ADA4938-2 ADC drivers are designed for applications that require more than one high performance ADC, such as in communications systems with I and Q sampling and in multichannel instrumentation. The devices have low input voltage noise (2.2 nV/√Hz) and low distortion, enabling design engineers to get the most out of their high performance ADCs. The adjustable level of the output common mode allows the ADA4937-2 and ADA4938-2 to match the input range of the ADC.

The ADA4937-2 works on a 3 V to 5 V supply range, and is specified to operate over the temperature range of –40°C to +105°C. The ADA4938-2 works on a 5 V to 10 V supply range and is specified to operate over the industrial temperature range of –40°C to +85°C. Both are available in a 24-lead LFCSP package. Single versions (ADA4937-1 and ADA4938-1) are also available.

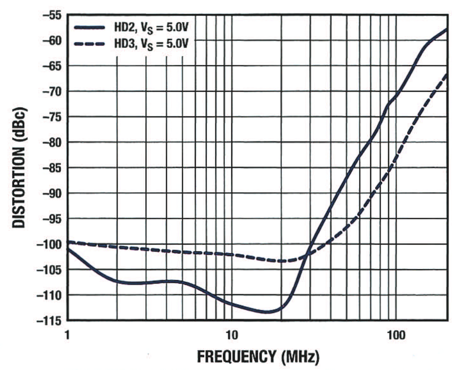
ADA4937-2

- –112 dBc/–102 dBc HD2/HD3 @ 10 MHz
- –79 dBc/–91 dBc HD2/HD3 @ 70 MHz
- –70 dBc/–84 dBc HD2/HD3 @ 100 MHz
- –3 dB BW @ 1.9 GHz, G = 1
- Slew rate: 6000 V/µs
- V_S = 3.3 V to 5 V

ADA4938-2

- –112 dBc/–102 dBc HD2/HD3 @ 10 MHz
- –79 dBc/–81 dBc HD2/HD3 @ 50 MHz
- –3 dB BW @ 1.5 GHz, G = 1
- Slew rate: 4700 V/µs
- V_S = 5 V to 10 V

DISTORTION vs. HARMONIC FREQUENCY



Online seminar on demand: "New Dimensions in Driving ADCs" at *www.analog.com/onlinseminars/drivingADCs*.

APPLICATIONS

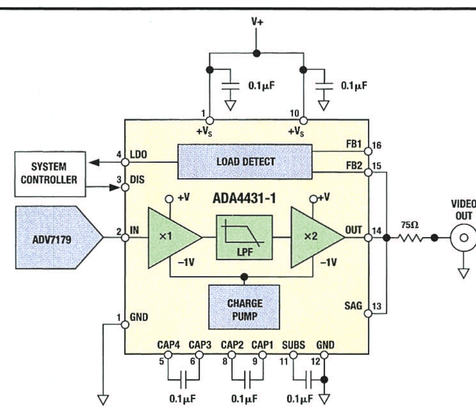
- Single-ended to differential converters
- High speed instruments
- IF and baseband amplifiers
- Differential buffers
- Line drivers

ADA4937-2	$5.59
ADA4938-2	$5.59
ADA4937-1	$3.79
ADA4938-1	$3.79

Feature-Rich, Volume-Priced Video Buffer Reduces Power and Size for Portable Applications

The ADA4431-1 video buffer includes a standard definition video filter, automatic load detect, and a charge pump. The device has a low quiescent current of 4 mA, and the load detect feature enables the system to turn on most circuitry only when a cable is connected. The charge pump reduces the need for a negative supply or a large ac coupling capacitor and internal filter—thereby eliminating large passive filter networks and the board space required. It is available in a 24-lead LFCSP package.

- 1 dB flatness out to 6 MHz
- Charge pump provides negative supply
- Low quiescent current: 4 mA typical
- Ultralow power-down: 0.1 µA typical
- On-chip load detection
- Low 0.55 mm package height



The ADV7179 is a chip scale NTSC/PAL video encoder with advanced power management features.

Online seminar available on demand: "Analog Filtering and Buffering for Video Applications" at *www.analog.com/onlinseminars/video-filter-buffer*.

APPLICATIONS

- Portable media players
- Portable gaming consoles
- Cell phones
- Digital still cameras
- Portable DVD players
- Portable video cameras

ADA4431-1	$0.39

High Voltage Precision Current Monitors for Industrial, Medical, and Automotive Applications

The AD8211 (single) and AD8213 (dual) precision current sense amplifiers feature a set gain of 20 V/V, with a maximum 0.5% gain error over the entire industrial temperature range of –40°C to +125°C. The buffered output voltage directly interfaces with the converter. Excellent common-mode rejection from –2 V to +65 V is independent of the 5 V supply. Special circuitry is devoted to maintaining output linearity throughout the input differential range of 0 mV to 250 mV, regardless of the common-mode voltage present. The AD8213 also features additional pins that allow the user to low-pass filter the input signal before amplifying via an external capacitor to ground. This part is fully qualified per the AEC-Q100 automotive standard. The AD8211 is available in a SOT-23 package, and the AD8213 is available in a 10-lead MSOP package. Both parts are ideal for applications such as motor control, solenoid control, battery management, and power supply monitoring.

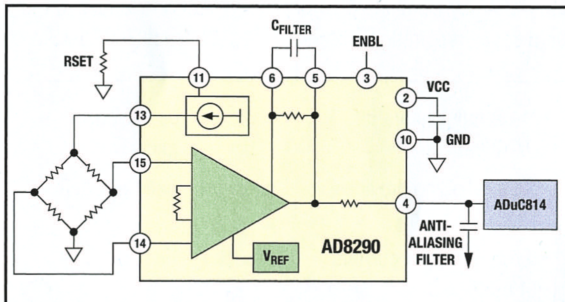
Part Number	Product Category	Common-Mode Range (V)	Input	Gain	Bandwidth	Input Impedance	Package	Price ($U.S.)
AD8202	Diff amp	–6 to +30	Unidirectional	20	50 kHz	200 kΩ	8-lead SOIC, 8-lead MSOP	1.35
AD8203	Diff amp	–8 to +28	Unidirectional	14	50 kHz	200 kΩ	8-lead SOIC, 8-lead MSOP	1.35
AD8205	Diff amp	–2 to +65	Bidirectional	50	50 kHz	200 kΩ	8-lead SOIC	1.35
AD8206	Diff amp	–2 to +65	Bidirectional	20	100 kHz	200 kΩ	8-lead SOIC	1.35
AD8210	Current sense	–2 to +65	Bidirectional	20	500 kHz	5 MΩ	8-lead SOIC	1.79
AD8211	Current sense	–2 to +65	Unidirectional	20	500 kHz	5 MΩ	5-lead SOT-23	0.80
AD8212	Current sense	+7 to +65	Unidirectional	Adj	500 kHz	5 MΩ	8-lead MSOP	0.92
AD8213	Current sense	–2 to +65	Dual, unidirectional	20	500 kHz	5 MΩ	10-lead MSOP	1.99
AD8214	Current sense threshold detector	+5 to +65	Threshold detection	N/A	200 ns prop delay	5 MΩ	8-lead MSOP	0.75

Low Cost, Integrated Bridge Sensor Conditioner Measures Sensors for Low Power Applications

The AD8290 contains both an adjustable current source to drive a sensor bridge and an instrumentation amplifier to amplify the signal voltage. The device is set for a fixed gain of 50. The AD8290 is an excellent solution for both the driving and sensing functions required for pressure, temperature, and strain gage bridges.

Because the AD8290 consumes minimal power, works with a range of low supply voltages, and is available in a low profile package, it is also well-suited for drive and sense circuits in portable electronics as well. The AD8290 is operational over the industrial temperature range of –40°C to +85°C.

- Supply voltage range: 2.6 V to 5 V
- Excitation current range:
  - 300 μA to 1300 μA
  - Set with external resistor
- Input bias current: 100 pA
- CMRR: 120 dB
- Package: 16-lead LFCSP, 3 mm × 3 mm × 0.55 mm
- Low power:
  - 1.2 mA + 2× excitation current
  - 0.5 μA shutdown current



AD8290

APPLICATIONS
- Bridge drive and sensor
- Portable electronics

$1.50

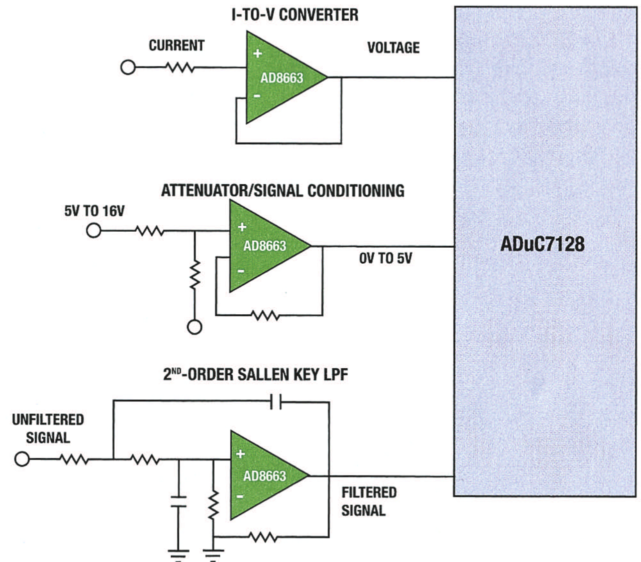
Online seminar available on demand:
"Options and Solutions for Sensor Signal Conditioning"
at *www.analog.com/onlineseminars/sensorsignals*.

Versatile 16 V Micropower Amplifier Available in LFCSP for High Density PCB

iCMOS INDUSTRIAL

The AD8663 amplifier is ideal for industrial and instrumentation applications that require tight signal chain error budgets where dc offset, voltage noise, accuracy over temperature (450 μV max at 125°C), and low bias current are important. The device is manufactured on ADI's *i*CMOS® process and offers guaranteed tested precision for both single supply (5 V to 16 V) and dual supply (±2.5 V to ±8 V). It is capable of supporting the high voltages required of lithium-ion and lithium-polymer batteries while also providing power efficiency, thermal management, and precision performance. The AD8663 is available in 8-lead LFCSP and 8-lead SOIC packages. The dual version AD8667 is also available.

- V_{OS}: 175 μV maximum
- TCV_{OS}: 1.5 μV/°C
- I_{SY}: 210 μA
- V_{SY}: 5 V to 16 V
- Voltage noise: 21 nV/√Hz



The ADuC7128 is a precision analog microcontroller ARM7TDMI® MCU with 12-bit ADC and DDS DAC.

AD8663 $0.64

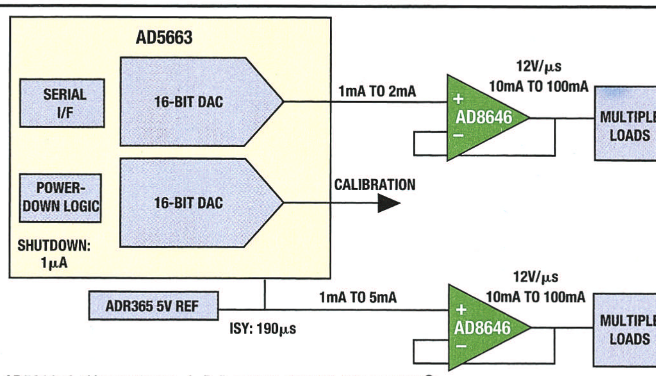
APPLICATIONS

- Portable instrumentation
- Mobile industrial controls
- Electrometers
- Photodiode preamps
- pH meters
- Ion detectors

High Performance Value in Versatile 24 MHz, Low Noise, R-R I/O Amp Family

The AD8646 and AD8647 are 2.7 V to 6 V rail-to-rail input/output amplifiers designed for a wide variety of applications that require wide bandwidth, a fast slew rate, low noise, and low bias current. The AD8647 also offers a low power shutdown function which, when enabled, draws 10 nA current maximum. In the example below, the AD8646/AD8647 are used as precision buffers to drive higher loads than what some converters and references can handle. The AD8646 is available in 8-lead MSOP and 8-lead SOIC packages. The AD8647 is available in a 10-lead MSOP package.

- Bandwidth: 24 MHz
- Slew rate: 12 V/μs
- Low noise: 8 nV/√Hz
- Low input bias current: 1 pA
- High output current: 150 mA



AD5663: 2.7V to 5.5V, 25μA, R-R output, dual 16-bit nanoDAC®
ADR365: low power, low noise, voltage reference, sink/source capability, $5.0V_{OUT}$

AD8646 $0.39*
AD8647 $0.45*
*at 100k unit

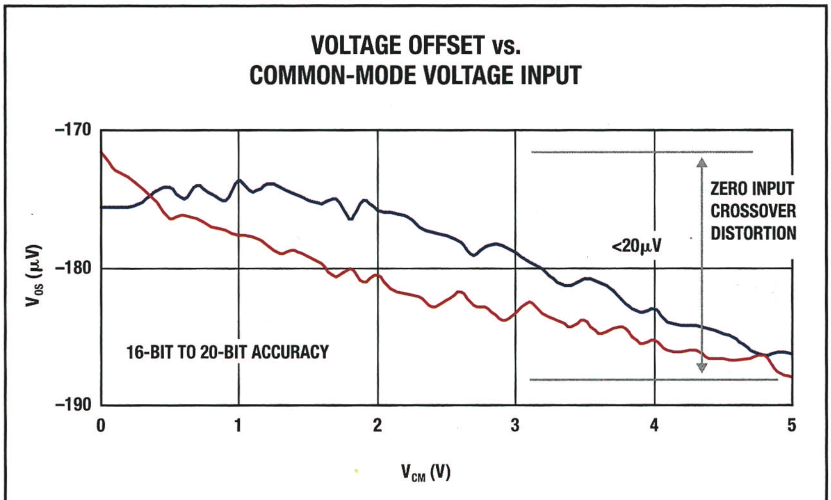
APPLICATIONS

- Reference buffering
- DAC buffering
- Audio preamps
- Charge amplifiers
- Photodiode preamp
- Filters
- Low noise gain amplifiers

5 V, Low Power, High Linearity, R-R I/O Amplifier Offers Zero Input Crossover Distortion

The AD8506 is a high performance, 20 μA, dual CMOS amplifier that boasts 105 dB CMRR. It maintains very high linearity over the entire input range. Zero input crossover distortion provides 16-bit to 20-bit accuracy, which is important in blood pressure and glucose meter measurements. It is currently available in an 8-lead MSOP package. An 8-lead WLCSP package is planned for release in early 2008.

- I_{SY}: 20 μA max
- CMRR: 105 dB
- PSRR: 105 dB
- Offset voltage: 2 mV
- Offset drift: <5 μV/°C



AD8506 $0.70

APPLICATIONS

- I-to-V converters
- Remote battery-powered sensors
- Handheld instrumentation
- Patient monitors
- Glucose meters
- Biological sensors

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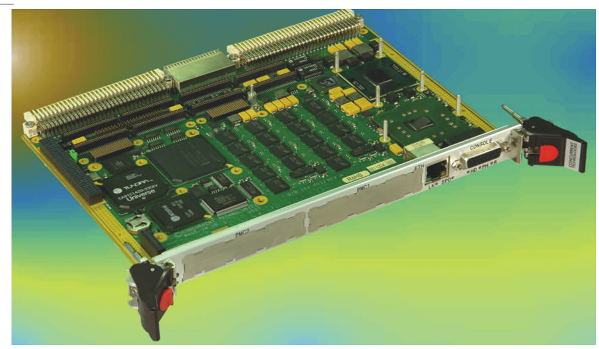
INNOVATIONS & INNOVATORS

Low-power VME board sports dual processors

Targeting low-power, computationally intensive applications within the defense, industrial-control, and transportation markets, Concurrent Technologies recently announced a single-slot VME single-board computer, which receives its power from the latest mobile dual-core processors from the Intel (www.intel.com) embedded-system lineup. The VP 417/03x supports either the 2.16-GHz Intel Core 2 Duo T7400 processor or the 1.5-GHz Intel Core 2 Duo L7400 processor, accessing as much as 4 Gbytes of SDRAM at speeds as high as 6.4 Gbytes/sec. The board supports VITA (VMEbus International Trade Association) 31.1 GbE (Gigabit Ethernet) on the VME64x backplane to enable high-speed board-to-board communications, improve application efficiency, and offload the standard VME backplane. VITA 31.1 is popular for applications such as data acquisition and radar data processing, as well as those requiring data synchronization across multiple system boards.

Providing two 66-MHz PMC (PCI-mezzanine-card) sites, the VP 417/03x also offers an array of I/O functions, including analog graphics and keyboard, mouse, RS-232/422/485, and USB interfaces. To support a variety of applications, the board includes 64 Mbytes of flash memory, an ATA (advanced-technology-attachment) 100 Enhanced IDE (integrated-drive-electronics) interface, and an onboard option for CompactFlash modules or a 2.5-in. disk drive. The VP 417/03x supports the Linux, Windows, Solaris, LynxOS, QNX, and VxWorks operating systems. Prices start at $4289.**—by Warren Webb**

▷**Concurrent Technologies**, www.gocct.com.



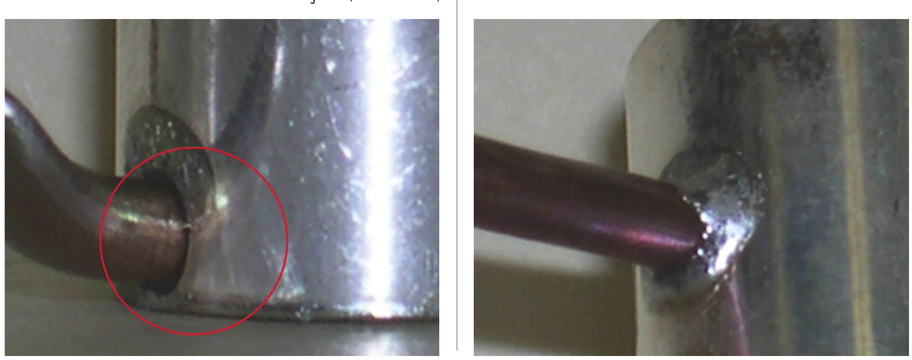
The VP 417/03x VME single-board computer offers designers dual PMC sites and high performance per watt using Intel's Core 2 Duo processors.

Humble solder paste enables exotic heat-transfer devices

EFD has introduced the nondrip SAC305 solder paste for gap filling and application on vertical surfaces in heat-transfer applications. Although news on this technology emphasizes the use of heat sinks, spreaders, and heat-wicking material, EFD's new paste deals with the assembly and mounting of these devices. Mounted vertically, these devices often can't do their jobs, because, during solder reflow, the paste drips down the device and disappears. The **photos** show a joint with insufficient solder due to flux dripping and a fully wet joint using EFD's paste, resulting in a solder flow around the heat tube.

—by Margery Conner

▷**EFD**, www.efd-inc.com.



Solder flux drips away from the heated vertical surface during assembly of a joint, preventing heat transfer along the heat tube (left). EFD's new paste helps create an effective joint, even on a vertical surface, enabling proper heat transfer (right).

Economical RF-vector-signal analyzer achieves top measurement speed

Agilent Technologies has introduced its EXA RF-VSA (vector-signal analyzer), which the company says sets a new standard for value in its field. According to Agilent, the EXA is the industry's fastest economy-class signal analyzer. Says a company spokesperson, the instrument's speed and accuracy, coupled with its unprecedented performance, application coverage, flexibility, scalability, and broad connectivity, provide development and manufacturing engineers with the capabilities to cost-effectively troubleshoot new designs; increase manufacturing throughput; and analyze complex, time-varying signals.

In combination with the manufacturer's 89600 VSA software, the EXA seamlessly integrates the same broad range of standards-based measurements at a lower performance point than that of Agilent's MXA signal analyzers. In addition, through the use of an open version of Microsoft's (www.microsoft.com) Windows XP Professional operating system, the EXA provides an advanced signal-analysis user interface, which intuitively groups all measurement functions and makes them accessible from the front panel or through a USB keyboard and mouse.

> "The intrinsic speed allows measurements as much as three times as fast as those of other economy-class units and is unprecedented in the class.

Optional measurement-application software provides preconfigured test routines for GSM (global system for mobile communication)/EDGE (enhanced data rates for global evolution), 802.16e Mobile WiMax, W-CDMA (wideband-code-division/multiple-access), HSDPA/HSUPA (high-speed-downlink/uplink-packet-access), and phase-noise applications. Running the 89600 software in the EXA enables advanced signal-demodulation analysis and troubleshooting of more than 50 demodulation formats, including 2G, 3G, 3.5G, WiMax, WLAN (wireless local-area network), and private mobile radio.

The EXA also includes a comprehensive set of standard one-button-power measurements for characterizing signal quality. These measurements include ACPR (adjacent-channel power ratio), channel power, occupied bandwidth, spectrum-emissions mask, CCDF (complementary cumulative-distribution function), burst power, and spurious emission. A key feature of the EXA is its intrinsic speed. According to Agilent, this speed, which allows measurements as much as three times as fast as those of other economy-class units, is unprecedented in the class.

The instrument family supports multiple frequency ranges from 9 kHz to 3.6, 7, 13.6, and 26.5 GHz. The 3.6-GHz unit offers an internal fully calibrated preamplifier option and provides a standard 10-MHz analysis bandwidth. This fully scalable capability complements the unit's −146-dBm/Hz displayed average-noise level without a preamp, 13-dBm third-order intercept, and 66-dB W-CDMA ACLR (adjacent-channel-leakage-ratio) dynamic range. And, thanks to the all-digital 14-bit-ADC IF (intermediate-frequency) section, the unit also has industry-leading 0.4-dB-maximum total-absolute-amplitude error. An optional 2-dB-mechanical-step attenuator maximizes the dynamic range over the full frequency range. A 1-dB electronic attenuator is optional on 3.6-GHz-bandwidth units.

The N9010A EXA signal analyzer fully complies with the LXI (LAN extensions for instrumentation) Class C instrument-packaging and networking specification. IEEE 488 and 100BaseT LAN ports and seven USB 2.0 ports provide connectivity. Prices begin at $16,900.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/exa.

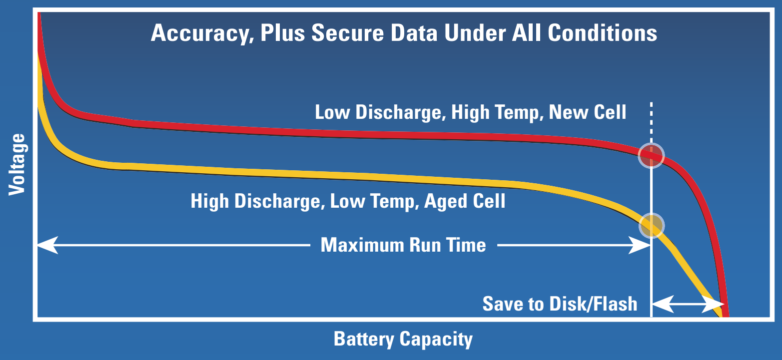
The economically priced EXA RF VSA is available with a bandwidth as great as 26.5 GHz. According to the manufacturer, the units set a new standard for measurement speed in economical VSAs.

DILBERT By Scott Adams

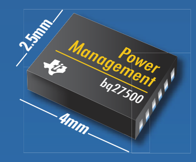
Run Smarter, Run Longer

System-Side Impedance Track™ Battery Fuel Gauge

The new **bq27500** system-side battery fuel gauge from Texas Instruments accurately predicts battery run time in smart phones and other handheld electronic devices. Featuring TI's patented Impedance Track technology, the IC maintains accuracy for the entire life of the battery under all conditions, reserves energy to save data and never sacrifices run time.



High-Performance Analog >>Your Way



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TEXAS INSTRUMENTS

PCIe Gen2 boosts lane rates to 500 Mbytes/sec

The second generation of PCIe (Peripheral Component Interconnect Express) technology is upon us with vendors planning new IC families and support chips. Meanwhile, PCIe 1.1 technology moves to enable embedded-system applications, and more highly integrated, low-power chips are set to debut. The PCIe Gen2 standard doubles the data rate possible in each lane of the scalable serial interface to 500 Mbytes/sec. As with the first generation of PCIe technology, designers can combine as many as 32 lanes to support escalating bandwidth demands.

PCIe found immediate adoption in connecting graphics cards inside PCs and has found use in servers and communications gear. The Gen2 technology will target similar applications. In applications other than those within a PC, a PCIe switch serves as the heart of the system architecture. PLX Technology has offered a broad line of PCIe switches in its PEX 8000 family and is now adding six Gen2 switches to the family. The new family includes switches with 12 to 48 lanes and three to 12 ports.

The ICs support load balancing and a dual-cast feature, which allows the switch to forward data to multiple output ports. PLX claims that flip-chip packaging maximizes signal integrity. Moreover, the switches can dynamically set lane rates and power down unused functional blocks to minimize power consumption. Typical system configurations range from the 32-lane, eight-port PEX 8632 in a workstation-graphics role to the 48-lane, 12-port PEX 8648 in a server-backplane-fabric role. Prices range from $25 to $75 (volume quantities), samples will become available in the fourth quarter of this year, and production units will become available in the first quarter of 2008.

IDT, which in the spring announced 12-lane, three-port and 16-lane, four-port Gen2 switches, has targeted low cost and low power with its latest announcement. The new PCIe 1.1 switches range from the three-lane, three-port 89PES3T3 to the eight-lane, five-port 89PES8T5A, and prices range from $7.60 to $12.80 (volume quantities). IDT claims that the new ICs are the industry's smallest PCIe switches and offers them in no-lead QFN packages. Target applications include automotive, medical, and consumer applications.

You can also expect support chips such as driver ICs for Gen2 to hit the market by the first quarter of next year. Pericom, for example, plans to ship a Gen2 version of its PCIe Re-Driver IC in that time frame.

—by Maury Wright

▷**IDT**, www.idt.com.

▷**Pericom**, www.pericom.com.

▷**PLX Technology**, www.plxtech.com.

Handheld cable-and-antenna tester focuses on field engineers, technicians

Agilent Technologies has introduced the handheld, battery-operated N9330A cable-and-antenna tester, which provides basic performance and optimized usability for installation and maintenance of wireless and cabled communication equipment. Covering 25 MHz to 4 GHz, the unit supports GSM (global system for mobile communication), CDMA (code-division/multiple-access), 3G, PHS (personal-handyphone-system), WLAN (wireless-local-area-network), military-communications, broadcasting, and radio links.

Although transceiver equipment is mature and stable, transmission lines are typically the most common failure points in a communication system. Cable-and-antenna systems face environmental elements, such as sun, rain, and wind, causing them to degrade over time. Poorly tightened connectors or seals can cause intermittent outages or even total failure. Cable-and-antenna testers are basic tools for installation, periodic maintenance, troubleshooting, and repair of these systems and are some of the most efficient tools for addressing these needs.

The N9330A, which makes frequency-domain and distance-to-fault measurements over its full frequency range, features long battery life, USB connectivity, a multilanguage user interface, and powerful postanalysis software. Despite being lightweight, the unit has a rugged design that enables it to withstand extended use under inhospitable field conditions. The power-saving, transreflective, 7.2-in., 640×480-pixel color LCD makes the readout easy to see in sunlight and in poor lighting. Fast calibration and a straightforward test procedure maximize the productivity of busy technicians.

The unit offers test accuracy on as many as 521 test points and supports three types of test-data points. Measurement speed is 3 msec per data point at full span with 521 test points in continuous-wave-speed mode. The device's rechargeable lithium-ion battery provides four hours of operating time, and the device has USB connections for both flash disks and PCs. The user interface supports traditional and simplified Chinese, English, French, German, Italian, Japanese, Korean, Portuguese, Russian, and Spanish languages. Prices start at approximately $7800.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/N9330A.

The N9330A's power-saving transreflective color LCD enables four-hour battery life yet permits easy viewing under a wide range of ambient-light conditions.

Multicore processor features 64 programmable cores

Tilera based its Tile64 processor on a mesh-multicore architecture that can scale to thousands of cores. The processor is the first silicon instantiation of the architecture, and it contains 64 programmable cores. Each core is a full-featured, general-purpose processor, including L1 and L2 caches, and each can run its own operating system, such as Linux. The cores connect to each other and the outside world through the iMesh (intelligent-mesh) network, which places a packet-communications switch on each processor core and arranges the cores in a grid fashion to enable low-latency, high-bandwidth communications between the cores, memory, and I/O.

The processor integrates four DDR2-memory controllers, two XAUIs (10-Gbps attachment-unit interfaces), two 10-Gbps PCIe (Peripheral Component Interconnect Express) interfaces, two 1-Gbps Ethernet RGMIIs (reduced-gigabit-media-independent interfaces), and a programmable flexible I/O interface to support CompactFlash and disk drives. The Tile64 processor targets infrastructure-video and -telecommunications applications. It can support two streams of broadcast-quality, high-definition H.264-encoding capability in a single chip and more than 10 streams of encoding for high-definition videoconferencing applications. The processor enables processing for as much as 20 Gbps of L4 to L7 telecommunications services.

The Eclipse-based integrated development environment supports an ANSI-standard C compiler, a full-system-simulation model, and a set of flexible command-line interfaces. The multicore-development environment provides graphically driven tools for debugging and profiling multicore processors as well as an application-level library that provides lightweight, socketlike stream-communication mechanisms. To leverage open-source tools and applications, the Tile64 processor supports a standard SMP (symmetric-multiprocessing) Linux programming environment. Three variants of the processor are available now, with prices starting at $435 (10,000), based on frequency and integrated peripherals. Tilera's road map also includes plans for 36- and 120-core devices.

—by Robert Cravotta

▷**Tilera**, www.tilera.com.

> The processor integrates four DDR2-memory controllers, two XAUIs, two 10-Gbps PCIe interfaces, and two 1-Gbps Ethernet RGMIIs.

FEEDBACK LOOP

"The RS-485 standard, with its continuously improving transceiver circuits, is and will be, with regard to industrial applications, the physical-layer standard for decades to come."

—Reader Thomas Kugelstadt takes a position on standards, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6459059. Add your comments.

FREE MULTISIM SPICE TOOL EASES ADI-BASED DESIGN

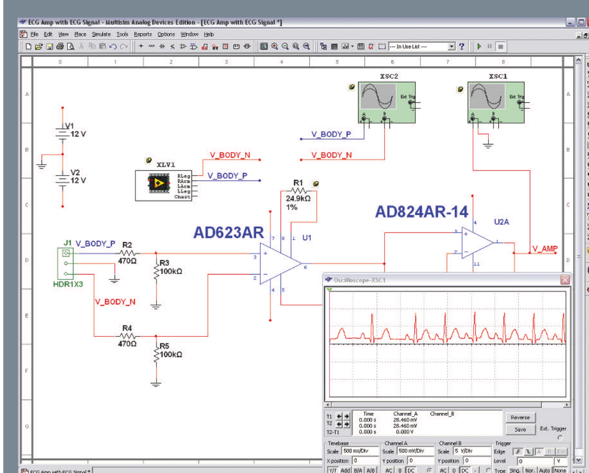
09.27.07

ADI (Analog Devices Inc) and National Instruments' Multisim group have teamed up to provide a free download of a special version of the Multisim SPICE tool that comes with models of ADI op amps and other linear components. The tool is most useful to designers who are comfortable with using the ADI product portfolio, although it would provide any designer with a way to quickly prototype a conceptual circuit. The NI Multisim Analog Devices Edition tool includes more than 1000 component models. ADI and National Instruments previously partnered to provide the ADIsimOpAmp online tool for parametric evaluation of op amps. You can download the tool at www.analog.com/multisim. The price for the complete version of NI Multisim starts at $1499.

—by Maury Wright

▶Analog Devices, www.analog.com.

▶National Instruments, www.ni.com/multisim.



This special version of the Multisim SPICE tool comes with models of Analog Devices op amps and other linear components.

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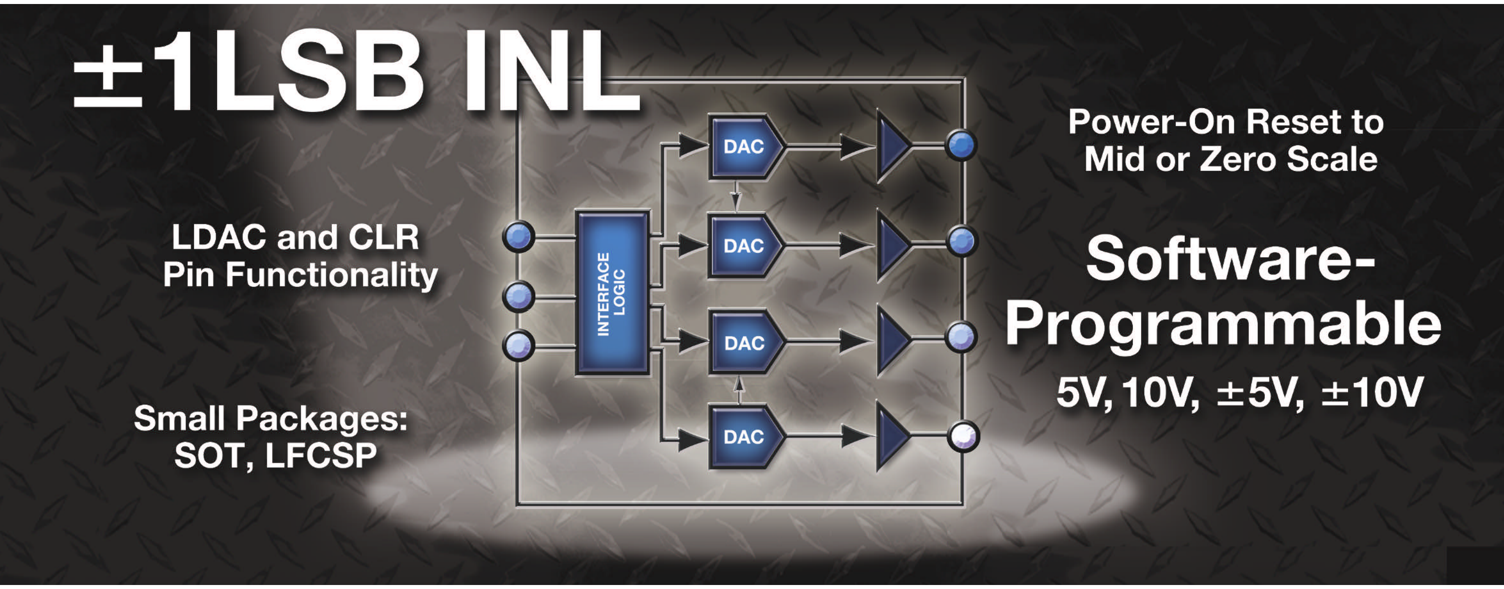

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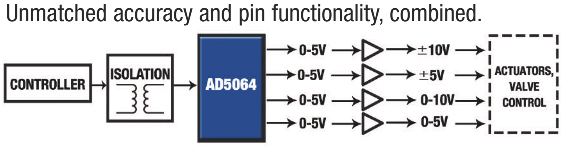
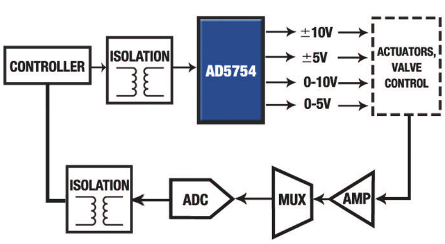


AD5754
Flexible Solution for Closed-Loop Systems

The AD5754 provides a software selectable output range of 5 V, 10 V, ±5 V, and ±10 V for cost-efficient system configuration.



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AD5764	Quad, ±15 V, ±1 LSB INL (max)	$35.70
Ideally Suited to Closed-Loop		
AD5752	Dual, software-programmable output range of 5 V, 10 V, ±5 V, ±10 V in 24-lead TSSOP	$6.95
AD5754	Quad, software-programmable output range of 5 V, 10 V, ±5 V, ±10 V in 24-lead TSSOP	$10.05
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ANALOG DEVICES

VOICES

Mark Wecht: Embedding high-performance technology

Mark Wecht is founder and chief executive officer of ESD (Embedded Systems Design, www.embedded-sys.com), where he and his engineering staff constantly push the technology envelope in high-performance embedded-signal-processing systems. ESD specializes in software-defined radio, beam-forming technologies, real-time streaming data, and FPGA-based software and hardware systems. Wecht earned a bachelor's degree in electrical engineering from Johns Hopkins University (Baltimore, MD) in 1992.

What are the common technical challenges that your customers face, and how does your company deal with them?

A The common technical challenges our customers face today are reducing size, weight, power, and the cost per data stream or channel of these processing systems. The problem is that a system usually costs more to build small, light, and energy efficient, which doesn't help the cost per channel. ESD Inc is currently working on methods of providing affordable scalability of FPGA-based technologies using standard networking technologies. Emerging lower power FPGAs coupled with Ethernet, Linux, and TCP/IP [Transmission Control Protocol/Internet Protocol] provide a highly scalable, affordable architecture for multistream- and multichannel-processing systems.

What is the potential for FPGA technology in high-performance products and systems?

A I believe that there is great potential for FPGA technology in high-performance products and systems. I think the tools are not here yet, but it won't be long before combined software/hardware-boundary solutions are more easily developed. I see a day when the compiler will understand which parts of the program to implement in software and which parts in reconfigurable hardware. I see a day when commodity motherboards have CPU and reconfigurable hardware side by side with an operating system that uses them both.

How has the trend toward multicore processors impacted your design and software-development activities?

A The trend toward multicore processors has not had any impact on our design and software-development activities other than speeding up our hardware synthesis. The majority of our customers are still asking us to port blade-server algorithms written in C to FPGA material or develop combined hardware/software-boundary functions within system-on-FPGA designs.

Can you summarize the career path that took you from student to chief executive officer?

A A graduate of the Baltimore Polytechnic Institute in 1976, I found a job as a wire man and fabricator building and installing shipboard-motor-control centers and switchboards for Seatronic Engineering. Using my wiring skills, I started working as an R&D technician in 1980 for Catalyst Research, performing wire-wrap and other functions for the engineers. They offered to pay for my education, and I enrolled at Johns Hopkins University, where I spent the next 10 years going part time to complete my bachelor's degree in electrical engineering.

I left Catalyst as an engineer in 1986. I moved to Intel Corp, where I worked as a training engineer until 1987, developing and teaching workshops in assembly-language programming and system-software programming for the 8085, 8086/88, 80286, and 80386 microprocessors. In 1987, I moved to Pace Inc to be a product engineer and designed and implemented a soldering/desoldering unit featuring digital closed-loop temperature control based on the 8051. I started work for Comtex Inc in 1989 as a software engineer, where I coded several ISDN [integrated-services-digital-network] protocols and a proprietary call-management system for the 68000 processor.

In 1992, I worked for a government contractor, Communications & Systems Specialists

Inc, as an embedded-software engineer. In 1995, I moved to TRW, where I spent one year while I prepared to start my own company. I founded ESD in 1996, and, for almost 12 years, I have provided the leadership, vision, and motivation to move ESD forward while continuing to contribute as an architect and systems engineer.

Can you offer any suggestions to students considering a career in engineering?

A I tell students considering a career in engineering to try to stay in school and go straight through to get at least a four-year degree before entering the work force. The further they can go straight through school, the better. I do urge that students involve themselves in cooperative or intern situations to get some real-life engineering experience. When I pick up a résumé of a student coming out of school with a bachelor's or a master's degree in engineering, I look first at the GPA [grade-point average] but quickly look for co-op or intern experiences.

—by Warren Webb

BY BONNIE BAKER

Reach out and touch

As the old AT&T slogan used to say, all you have to do is pick up a phone to "reach out and touch someone." Even for engineers, something as simple as this type of analog conversation can immediately clarify the most confusing details. There are times, however, when a phone conversation isn't enough. In these cases, maybe a picture is worth *more* than 1000 words. Enter the user-friendly touchscreen.

Imagine drawing a picture of your latest circuit creation on the screen, in real time and by hand in the analog domain. Then, immediately electronically send the picture to other interested parties. Although the touchscreen interface may be digital, the human interface is purely analog. With a touchscreen, you are converting the analog human touch into digital code.

Consumer-product designers can choose their touch panel from various technologies. Most available panel technologies use resistive, capacitive, SAW (surface-acoustic-wave), or IR (infrared) techniques. The most popular touchscreen on the market is resistive, because it is inherently stable and affordable.

There are four-, five-, seven-, or eight-wire resistive touchscreens. The most common resistive touchscreen has four wires. The layers of a four-wire resistive-touchscreen panel are a rectangular, flexible top layer; a transparent conductive-coated layer of ITO (indium-tin-oxide) material; air-gap and isolation spacers; another transparent ITO layer; and a stable layer (**Figure 1a**). The panel's flexible top layer (not shown) will flex enough, allowing a depression so that the two conductive layers can touch. Unless you apply pressure, the nearly invisible layer of spacers keeps the two ITO conductive layers apart.

When you touch the flexible top layer with a stylus or a finger, the pressure causes the two ITO layers to connect. While you are touching the panel, you apply power to one of the two ITO layers through the silver-ink conductive bars at opposing ends of that layer. When you power one ITO layer, such as the yellow layer in **Figure 1a**, you use the other ITO layer (green in the **figure**) to probe the location of the stylus by using a high-impedance successive-approximation-register ADC. The ADC converts the voltage that the stylus touch creates from the unpowered layer to a digital value.

For example, if you power the X layer from X+ to X− (yellow) with 2.5V and touch a stylus approximately one-third of the way between the two X-axis conductive bars, the voltage on the Y+ and Y− terminals (green) equals 0.833V. This voltage is proportional to the applied voltage across X+ and X−—a result of the resistive voltage divider of the panel (**Figure 1b**). You sense the Y position when you apply power to opposing conductive bars on the Y layer. You then use the X+ or X− terminals to sense the Y position of the stylus with the ADC.

In this manner, the simple resistive touch panel allows you to reach out and touch across the room or around the world.EDN

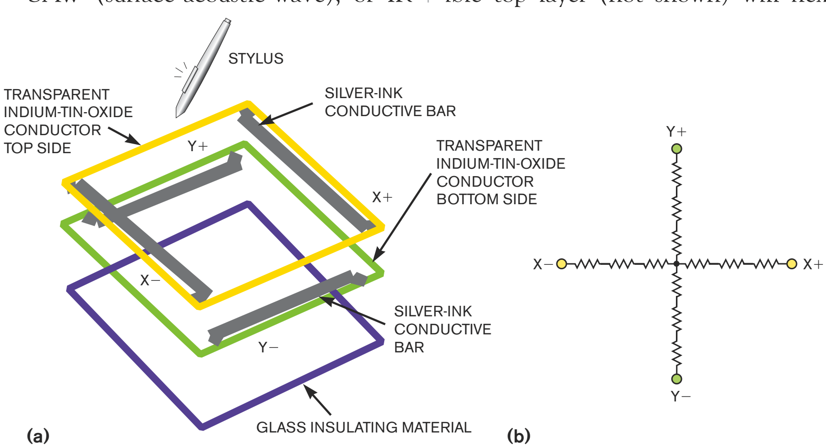

Figure 1 With the four-wire touchscreen panel, the two active areas of the resistive touchscreen sense the X and Y pressure points (a). The equivalent circuit is simply a voltage divider (b).

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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 BY WALTER LINDENBACH • CALGARY CONTROLS LTD

Time bomb

DANIEL VASCONCELLOS

There is a failure mode that is worse than intermittent; no tests, measurements, or parts replacement will directly reveal the cause. You can test the circuit on the bench and in the field for months, and it will work perfectly. Then, within a year, a transistor fails. When you replace it, the device works well for months; then, the same transistor fails again.

I once had to fix an oil-pipeline-monitoring device with a relay driver that behaved this way. One after another, the transistor that switched the relay coil would fail within a year of installation. The relay-coil resistance was about 240Ω (12V dc at 50 mA)—by no means an excessive load for a small TO-92 transistor.

But a little 12V relay coil can produce a 200V spike. I was amazed when I saw it for the first time, and, with the scope that I had 30 years ago, it was hard to see. A transistor was switching a relay coil at about 10 times per second, and the scope triggered on the leading edge of the collector voltage. I turned the beam intensity to maximum, readjusted the focus, and, finally, after turning off the room lights, saw something going off the top of the screen! By turning the vertical sensitivity down and down again, the peak of the spike was finally visible—at 200V! That voltage was probably the transistor base-emitter-breakdown limit, not the peak of the inductive-voltage spike. A transistor with a collector-to-emitter breakdown voltage of 80V will not last long under those conditions, and, if you don't protect it from the inductive spike, the transistor will fail after some number of switching operations—in minutes or months.

The usual way to protect a transistor from inductive spikes is to place a diode across the inductive load (cathode to V_{CC}). Such an arrangement slows the relay release, but this circuit had no speed requirement so would have been satisfactory.

But I think the designer had placed a 10-nF capacitor from the transistor collector to ground to suppress the inductive spike, thus perpetrating another failure mode that looks exactly like the inductive-spike-failure mode—*invisible*! Only the transistor collector's on-resistance and the resistance in the capacitor when the transistor switches on limit the current. Now, instead of an inductive-voltage spike, there is a capacitive-current spike, the amplitude of which is independent of the capacitor size. The current spike produces approximately the same result to the transistor as the voltage spike: It continues to operate for some time and then shorts.

I decided to protect the transistor with a different modification: I placed a 12Ω resistor in series with the emitter to limit the collector-current worst-case peak to 1A. A small plastic transistor, such as the MPS8099, can easily tolerate such a peak if it is short. Then, with a 50-mA normal relay-coil current, the drop across the emitter resistor was only 0.6V, which did not alter the performance of the circuit and seemed less likely to cause repercussions than removing the capacitor and adding a diode.

Now the monitoring device worked reliably. There were no more relay-driver failures to cause users to return these units for repair. **EDN**

Walter Lindenbach started and operated Calgary Controls Ltd from 1970 to 1990, at which point he discovered an allergy to work and retired. Like Walter, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

R A Q ' s

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Resistor Noise can be Deafening, and Hard to Reduce

Q. My low-noise amplifier is not low noise enough. What am I doing wrong?

A. It may not be the amplifier causing the trouble; analyze where the noise is actually coming from. A typical operational amplifier circuit contains six uncorrelated noise sources (the smaller ones can usually be disregarded[1]). The amplifier itself has three separate noise sources: a voltage noise source appears differentially across the inputs; and current noise sources appear in series with both inverting and non-inverting inputs. Remarkably often the problem is not the amplifier, though, but the thermal noise generated by one or more of the three resistors that set the amplifier gain and provide bias current compensation. Analog Devices has over sixty types of op amps whose voltage noise is less than that of a 1 kΩ resistor ($4\ \mathrm{nV}/\sqrt{Hz}$).

This answer is rarely popular; it is far more satisfactory to blame an imperfect amplifier and replace it with a better one than to admit that there is a fundamental problem with apparently simple components such as resistors. In fact, a remarkably common response to a diagnosis of resistor noise is to seek a source of ***"good"*** resistors, with ***"good"*** being defined as without thermal noise.

This is impossible. The basic physics of resistance shows[2] that the random thermal movement of charge carriers in a conductor always produces electrical noise of value $\sqrt{4kTBR}$ where k is Boltzmann's Constant (1.38065 x 10^{-23} J/K), T is the absolute temperature, B is the bandwidth and R the resistance. (We often express this noise in terms of spectral density, making the voltage noise $\sqrt{4kTR}\ {}^{V}\!/\!_{\sqrt{Hz}}$).

Such noise is known as thermal noise, or Johnson noise, after John B. Johnson (Bell Telephone Laboratories – 1928), who was the first person to observe it. It might more properly be named Johnson/Nyquist noise as it was Harry Nyquist (also at Bell Laboratories) who explained the physical basis of Johnson's observation.

So anywhere at all that there is resistance in a circuit, whether it is carrying current or not, there is a noise generator with an output voltage noise spectral density of $\sqrt{4kTR}$. We can reduce the noise by reducing the resistance (this may increase current and/or power consumption), but reducing the temperature is not usually practicable (if we cool a resistor from room temperature (298K) to liquid nitrogen temperature (77K), its noise voltage is still more than half its room temperature value). And, of course, we can't change Boltzmann's Constant because Professor Boltzmann is dead[3].

---

[1] *Any noise source less than ⅓ the magnitude of the largest can be ignored for most practical purposes.*

[2] *http://www.physics.utoronto.ca/~phy225h/experiments/thermal-noise/Thermal-Noise.pdf*

[3] *Died 5 September 1906 at Diuno near Trieste, buried Zentralfriedhof, Vienna.*

To learn more about noise,
Go to: http://rbi.ims.ca/5404-101

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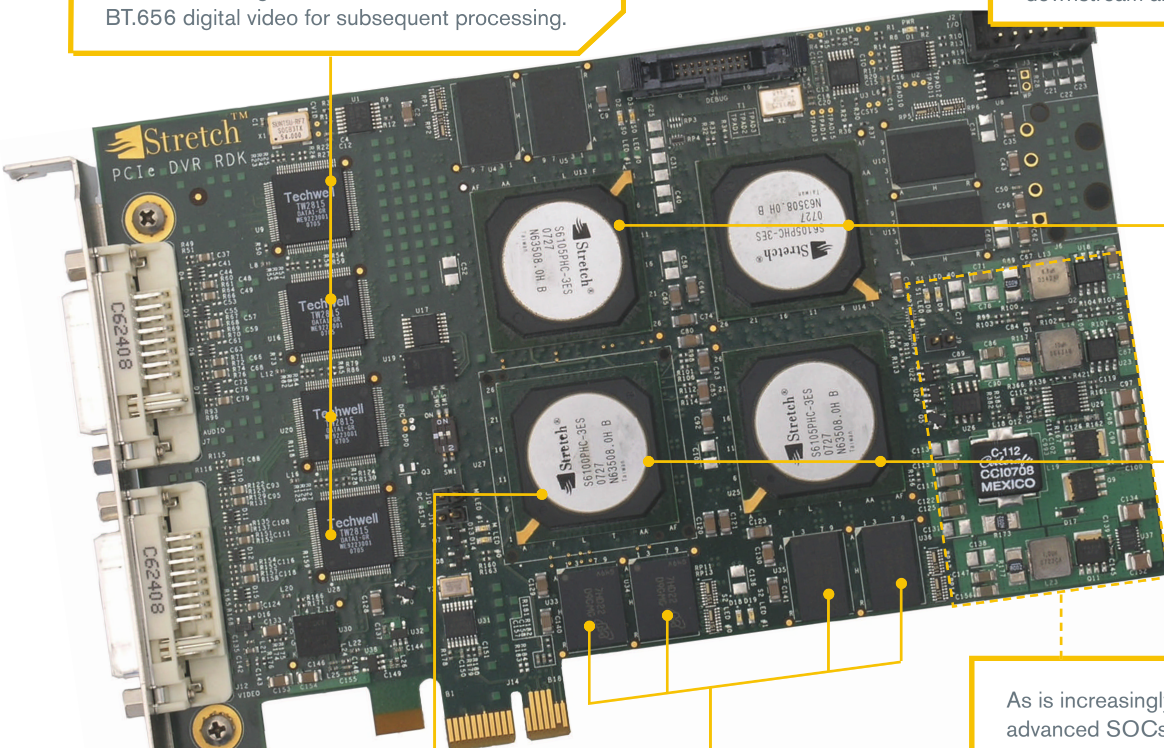
Visit www.edn.com/070927pry for an extended version of this article, including additional technical details and block diagrams.

Video surveillance: It's all about computing power

Placing an area under video surveillance means setting up lots of cameras. But that's the easy part. The system must concentrate the signals from those cameras for transmission back to a central hub, using as low a bit rate as possible, especially if the link uses Internet Protocol. Often, because most of the signals will go into storage unexamined by humans, software must refine the images, select potentially important ones, and even recognize objects or persons in the incoming video stream. All of these circumstances turn the surveillance-camera-electronics job from a simple task for a JPEG encoder into a serious image-processing load worthy of an array of programmable SOCs (systems on chips). A design that can handle this transformation is just what Stretch Inc has brought to the problem with its PCI Express DVR RDK reference-design board.

Four Stretch S6100s compress the incoming video using a software-based multistandard compression engine. Each device works on four channels, with one doubling as a supervisor. The chips working together are capable of H.264 D1 resolution encoding at 30 frames/sec on each channel. Significantly, there is processing room left over for video analytics that can scan images for content, adjust cameras or compression rates, or provide raw data for downstream algorithms.

The board uses four Techwell TW2815s to gather 16 video and 16 audio channels. These four-channel devices acquire NTSC/PAL composite video and analog audio, filter it, and convert it to BT.656 digital video for subsequent processing.



Stretch designed the board to use PCI Express as its means of communication with a host processor, which would save the compressed video locally or transmit it to a remote hub. The S6100 chip directly supports the interface.

Each Stretch chip uses a pair of Micron D9GMG DDR2 DRAMs for local storage in addition to the SRAM on the S6100 dice.

As is increasingly the case with advanced SOCs, the power-supply circuitry consumes nearly as much space as the computing heart of the board. The design must support the needs of the computing chips, DDR2 DRAMs, and analog front-end devices.

FLASH MEMORY'S PER-MEGABYTE COST IS PLUMMETING, AND ITS PER-CHIP DENSITY IS CLIMBING. YOUR CUSTOMERS' DEMANDS FOR SYSTEM PERFORMANCE, LOW POWER CONSUMPTION, COMPACT FORM FACTORS, LIGHT WEIGHT, RUGGEDNESS, AND RELIABILITY ARE UNRELENTING. IS IT TIME TO CONSIDER AN UPTICK IN YOUR PER-SYSTEM SOLID-STATE-CAPACITY BUDGET?

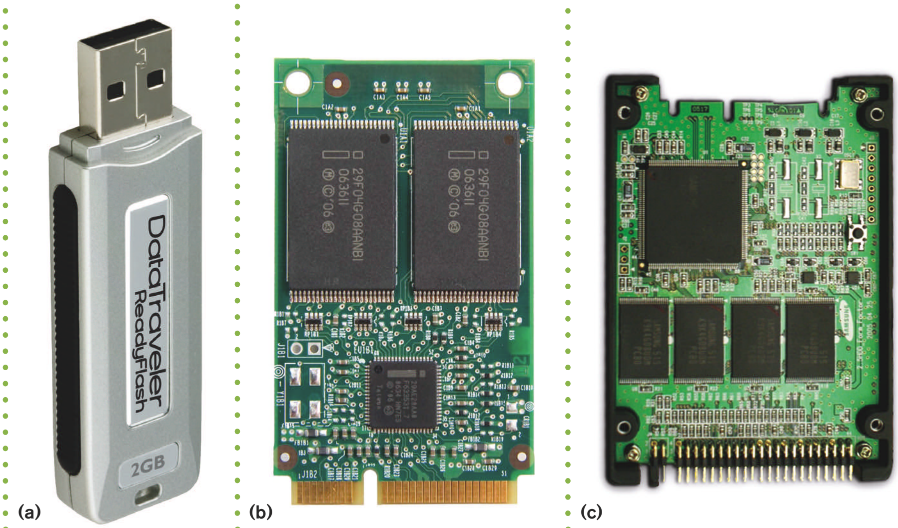


Figure 1 USB add-on "sticks" (a), embedded mini-PCI Express modules (b), and solid-state drives (c) are three of the many ways that high-density flash memory is muscling into computing platforms (courtesy Kingston, Intel, and Samsung, respectively).

SOLID-STATE STORAGE: FEASIBLE PLAN OR FLASH IN THE PAN?

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

Flash memory gained its first foothold in the PC architecture in 1991 with manufacturers' adoption of user-upgradable BIOS as a successor to ROM- and EPROM-based predecessors. Since then, incremental flash-memory-usage success has come through the use of solid-state-storage modules in a variety of form factors and system interfaces: USB, PCMCIA, CompactFlash, Secure Digital, and others. However, unlike BIOS, these additional flash-memory beachheads have been predominantly transitory, with users employing the solid-state storage as backup for the primary system hard-disk drive, for example, or as a means of interchanging data between two PCs or between a PC and another system, such as a PDA or a digital camera.

Over the past several years, however, industry interest has blossomed and accelerated in boosting the amount of flash memory in a system from multiple megabits to multiple megabytes—and even to tens of gigabytes (**Reference 1**). The flash-memory suppliers have to some degree cultivated this density-expansion attention; with the flattening out of consumer demand for traditional, high-density-flash-memory applications, such as cell phones, digital cameras, and PDAs, and with substantial incremental flash-memory supply becoming available, the memory vendors are eager to cultivate new markets (**Reference 2**). Hard-drive suppliers, similarly, are looking to augment—but not necessarily replace—their products with flash memory. They see this augmentation as a means of differentiating—and thereby garnering incremental revenue and, they hope, profits from—what has otherwise become a highly commodity-based rotating-magnetic-storage business.

Microsoft, too, is leveraging its Windows Vista's embrace of high-capacity flash memory in multiple implementation variations as a means of encouraging consumers to adopt the company's latest operating-system version. Supply-side cynicism aside, computer users *can* garner a number of potential advantages by migrating to high-density-flash-memory-inclusive computers. Those of you who are designing and using embedded systems may already be aware of—and exploiting—these advantages (see **sidebar** "Non-PC applicability").

AT A GLANCE

- Operating-system enhancements enable flash memory to act as a hard-disk-drive cache, an attractive scenario when you cannot upgrade the system's DRAM allocation.
- More encompassing caching support, supporting system-boot and return-from-hibernation scenarios, comes both integrated within the hard-disk drive and in external-to-hard-drive flash memory.
- Replacing magnetic rotating storage with a solid-state alternative is cost-effective only if your required amount of flash-memory storage is below the price "floor" of the hard-drive alternative.
- Regardless of the high-density flash-memory implementation, availability and cost concerns bear careful consideration before you proceed.
- Embedded systems have in many cases already blazed the hard-disk-drive-to-solid-state-drive trail that computers are now beginning to traverse.

READYBOOST ME?

From Microsoft's earliest DOS days with the SmartDrive utility, the company has striven to employ semiconductor memory as a fast cache for the slower hard-disk drive behind it. Until the emergence of Windows Vista, DRAM was the only applicable cache-technology candidate, and each incremental Windows version improved the effectiveness of that cache. Vista's SuperFetch is the most recent iteration of Windows' precaching. Its improvements over the Windows XP-based predecessor include built-in intelligence that suppresses the effects of background tasks, such as hard-disk-drive-backup and virus-scanning sessions, that might otherwise result in unnecessary and undesirable cache "thrashes." SuperFetch, according to Microsoft, can also "learn" from and adapt its behavior to a user's PC-operating patterns, not only for global-program preferences, but also for more finely grained time-of-day and day-of-week tendencies.

However, as Microsoft's Web site notes, "Adding system memory (typically referred to as RAM) is often the best way to improve a PC's performance, since more memory means more applications are ready to run without accessing the hard drive. However, upgrading memory can be difficult and costly, and some machines have limited memory-expansion capabilities, making it impossible to add RAM" (**Reference 3**). As a result, Windows Vista's SuperFetch supports hard-disk-drive caching not only to traditional DRAM, but also to supplemental flash memory, which requires no power-consuming constant refreshing as DRAM does. The company has tagged this approach with the ReadyBoost marketing moniker. This memory may reside on the motherboard. Examples of this approach include Intel's (formerly, Robson Technology's) Turbo Memory mini-PCI Express module and AMD's HyperFlash array. Alternatively, ReadyBoost can take the form of an add-in module. Thanks to SuperFlash's built-in, lossless 2-to-1 average compression and AES (Advanced Encryption Standard)-128 algorithm, Microsoft's hard-disk-drive-caching scheme makes secure and efficient use of the available flash-memory storage.

If you're thinking that all this news sounds too good to be true, here are a few caveats. Windows Vista discards information cached in a removable flash module upon exit from system hibernation, because the operating system can't tell whether the user has ejected the module and, therefore, potentially altered its contents during the system's hibernation interval. Flash memory's read and, especially, write performance is slower than the DRAM-implemented cache alternative. Random reads from

NON-PC APPLICABILITY

The magnetic-to-solid-state-storage trend is old news to those of you in noncomputer applications who have lived through the transition by virtue of the fact that, for example, your equipment's storage requirements are far less substantial than those of a PC. A dual-flash-memory-technology combination is one common system-implementation approach, employing a NOR device for initial boot code and NAND-flash memory as a solid-state drive. Either a dedicated hardware controller or flash file-system software from Datalight or another vendor manages these NAND devices.

If you prefer to boot directly from a NAND-flash memory, you must comprehend potentially "known-bad" blocks in your system memory-mapping scheme. Designers tolerate these blocks because they boost the effective device yield. You also must compensate for the fact that NAND-flash memory's random-access latency is longer than that of NOR devices. Some NAND-flash memories embed a small SRAM array along with a NAND-to-SRAM autotransfer controller and system-microprocessor hold-off-control signals. Alternatively, you can implement a NAND-to-NOR control-signal translator and wait-state generator in a discrete PLD, an FPGA, or another logic device (Reference A).

REFERENCE

A "QuickLogic Storage Solution Portfolio Runs the Gamut with Addition of NAND Flash Controller," QuickLogic, Feb 5, 2007, http://ir.quicklogic.com/releasedetail.cfm?ReleaseID=228315.

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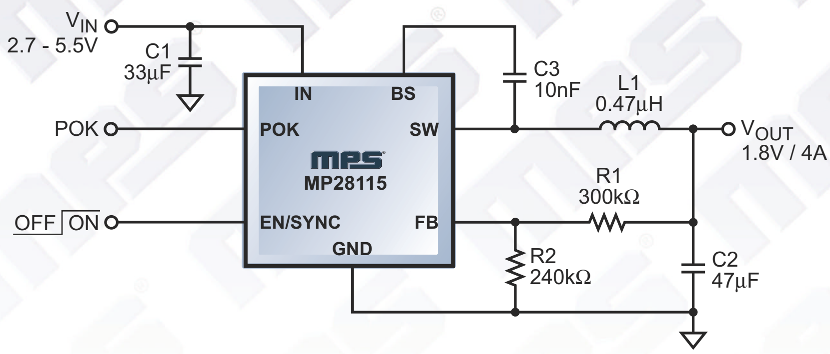

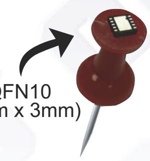

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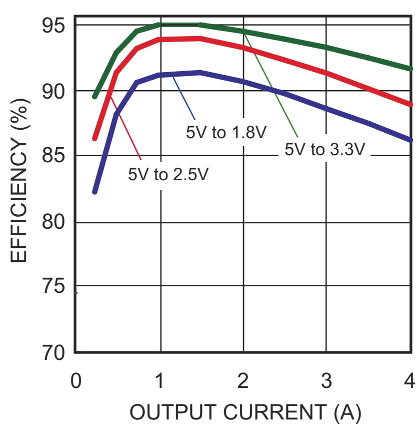

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flash memory, by virtue of their avoidance of rotating storage's rotational and seek latencies, are faster than those from a hard-disk drive. However, sequential-read-performance comparisons, along with both random- and sequential-write-performance evaluations, don't obviously favor flash memory. These assessments may, in fact, tip the scales in the hard-disk drive's favor, depending on the two technologies' system interfaces and the amount and effectiveness of the hard drive's built-in buffer RAM. As a result, Microsoft requires flash memory for ReadyBoost to satisfy stringent capacity and speed criteria, and Windows Vista won't activate a flash-memory module for ReadyBoost use unless the OS detects that the flash memory satisfies the following conditions (**Reference 4**):

- USB flash drives themselves and the host controllers into which you insert them must both use the USB 2.0 standard.
- USB flash drives must have at least 230 Mbytes of free space.
- Flash-storage devices must meet minimum performance requirements to support ReadyBoost, including 2.5-Mbyte/sec throughput for random 4-kbyte reads and 1.75 Mbytes/sec for random 512-kbyte writes.
- Devices must meet higher performance requirements to achieve the "enhanced-for-ReadyBoost" designation. These requirements are 5 Mbytes/sec for random 4-kbyte reads and 3 Mbytes/sec for random 512-kbyte writes. Microsoft recommends that users employ enhanced-for-ReadyBoost devices to take full advantage of the benefits ReadyBoost provides.
- ReadyBoost can support devices with cache sizes ranging from 230 Mbytes to 4 Gbytes. Microsoft recommends at least a 1-to-1 ratio of ReadyBoost cache size to main memory (RAM) capacity. Ratios as high as 3-to-1 realize the optimal performance benefits.

TABLE 1 READYDRIVE-PERFORMANCE REQUIREMENTS

Scenario	Sustained throughput (Mbytes/sec)
4-kbyte random reads to a file pinned in the nonvolatile cache	More than 4
4-kbyte random writes to a file pinned in the nonvolatile cache	More than 4
64-kbyte sequential reads to a file pinned in the nonvolatile cache	More than 16
64-kbyte sequential writes to a file pinned in the nonvolatile cache	More than 8

Although many flash-memory "sticks" meet Microsoft's ReadyBoost requirements, they're inconvenient and unaesthetic for constantly in-use hard-disk-drive-caching purposes because they protrude from the front, back, or side of the computer, depending on where its USB ports reside. Alternatively, Secure-Digital, ExpressCard, and other memory-card formats provide a means of safely cradling the ReadyBoost device within a computer's integrated card-reader slots. For desktop PCs, motherboard-resident USB connectors provide self-contained-system routes to implementing ReadyBoost. And mini-PCI Express connectors are also ReadyBoost candidates for both mobile and desktop computers. However, by populating these connectors with flash memory, you preclude their use for wireless connectivity or other functions. This issue is of particular concern with limited-I/O chip sets or small-form-factor motherboards, because both factors preclude the inclusion of more than one mini-PCI Express slot.

Theoretical capabilities aside, the near-term prognosis on ReadyBoost is mixed at best, although Microsoft released Windows Vista patches just before this article went to press. Those patches may more definitively deliver the performance boost that Microsoft has been promising for several years now. The ReadyBoost algorithms strive to take maximum advantage of flash memory's strengths and circumvent nonvolatile semiconductors' limitations. To do so, Microsoft's engineers tuned the ReadyBoost code using research-defined assumptions about how consumers typically use computers. If a given tester's synthetic or "real-life" benchmark radically detracts from Microsoft's vision by extensively writing to the hard drive, for example, ReadyBoost's improvements will be less evident than they would be otherwise, and, in the worst case, the system may even run more slowly with ReadyBoost turned on (see **sidebar** "Additional materials and a hands-on test-drive"). From the numerous ReadyBoost-testing results I've perused so far, four key conclusions regularly appear:

- ReadyBoost-performance improvements are most evident in mobile-computing environments, which tend to use slower hard drives than their desktop counterparts as a means of reducing power consumption.
- ReadyBoost particularly shines from a power standpoint with mobile PCs, because the scheme enables the hard drive to remain in its lowest power state more often. Conversely, with ac-powered desktop PCs, power consumption is generally less of a concern (see **sidebar** "Booting beyond BIOS?").
- By virtue of a SuperFetch cache, ReadyBoost "parks" the hard-drive head and spins down the platters for a higher

ADDITIONAL MATERIALS AND A HANDS-ON TEST-DRIVE

For more information, visit the Brian's Brain blog (www.edn.com/briansbrain) and peruse the solid-state-storage entries. You'll find online and print resources that can further expand your education on the topic, as well as an in-depth discussion on the supply-versus-demand influence on the market's evolution. I also showcase compelling commentary from industry representatives, including suppliers, users, and observers. And, as time allows, I also hope to include my real-life benchmarking results of solid-state drives versus hard-disk-drive competitors. To date, Samsung, Sandisk, and Super Talent have all promised me solid-state-disk-evaluation units.

percentage of the time, and the average operating temperature of the hard drive is therefore lower than it might be if a cache wasn't present. These factors tend to improve a hard-disk drive's overall ruggedness and reliability.

• If you can easily and cost-effectively upgrade your system with more DRAM, do so. DRAM delivers superior SuperFetch results to the supplemental-flash-memory alternative.

WILL READYDRIVE THRIVE?

Add to ReadyBoost the ability for the information stored in the flash-memory cache to survive system shutdown and hibernation cycles. Simplistically speaking, this augmented result is the concept behind ReadyDrive, another first-time Windows Vista capability. As Microsoft's documentation points out, ReadyDrive also offers hardware and software suppliers, as well as the SuperFetch algorithm itself, the ability to "pin" a given program or set of files such that the flash-memory array never flushes the pinned information. And, speaking of flushing, an operating system must support an expanded ATA (advanced-technology-attachment) command set to fully exploit a ReadyDrive-supportive storage subsystem. In Microsoft's words, "ReadyDrive uses a new NV [nonvolatile] cache command set standardized in the ATA8-ACS command specification. This new command set allows ReadyDrive to do two important things: control what data is pinned for retention in the NV cache at any given time and control whether the drive is put into the NV cache power mode."

The ReadyDrive-supportive storage subsystem can take one of two primary forms. The members of the Hybrid Storage Alliance support the inclusion of flash memory within the hard drive, supplementing the RAM buffers in today's drives. Conversely, Intel with Turbo Memory and AMD with HyperFlash advocate a flash-memory array outside the hard-disk drive. This external implementation works with a software driver that intercepts commands that would normally go to the hard drive and appropriately directs and otherwise handles them, cognizant of the nonvolatile-semiconductor-memory alternative. Both sides of this contentious platform tug of war make compelling arguments for their preferred techniques.

Hybrid-drive advocates suggest that the company that implements the hard drive can best manage the flash-memory cache, so that the two technologies can operate as synergistically as possible. They also point to the all-in-one simplicity of the hybrid-drive approach, which, among other things, negates the necessity of installing and maintaining

BOOTING BEYOND BIOS?

Solid-state storage consumes less power than rotating magnetic storage, making the solid-state approach a compelling fit in battery-inclusive systems. Solid-state drives' advantages are less obvious in ac-powered gear, because power consumption is less of a concern in such equipment—except, perhaps, in servers—and such systems also often embed higher performance hard-disk drives, in many cases including multidrive RAIDs (redundant arrays of inexpensive disks). Desktop, workstation, and server PCs also tend to have significantly higher storage-capacity requirements than their mobile brethren, thereby notably delaying the point at which solid-state disks will become cost-competitive on a dollar-per-gigabyte basis.

However, the emergence of operating-system virtualization in the computing platform creates another compelling opportunity for high-density flash memory. In this case, it would act as a "super BIOS," storing an in-system-upgradable "hypervisor" that would subsequently launch and act as an arbiter between multiple virtual-machine images on a hard-disk drive. Rumors are circulating that Dell is working on just such a configuration, and it will be interesting to see how widespread the implementation becomes in the future.

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a custom-software driver. It also precludes the potential for remnants of valuable stored information to remain accessible within the system after removal of the hard drive. Intel Turbo Memory advocate Rick Coulson admitted at May's WinHEC (Windows Hardware Engineering Conference) that such a scenario was possible but suggested that you could deal with this issue by automatically reformatting or otherwise "wiping" the hard drive, which also scrambles the Turbo Memory contents, before removing it. Intel plans to mitigate this problem in the future by encrypting the information stored in the Turbo Memory array.

INSTEAD OF SUPPLEMENTING THE HARD DRIVE WITH FLASH MEMORY, YOU MIGHT INSTEAD CHOOSE TO REPLACE IT WITH A SOLID-STATE DRIVE.

Supporters of implementing ReadyDrive in the external flash-memory array focus on the approach's flexibility in system design and supply sourcing, a compelling pitch in the current era of uncertainty about flash-memory cost and availability. A computer manufacturer can keep buying the same few hard-drive variants it always has without further complicating its supply chain with hybrid-drive options in multiple capacity, performance, and other variations. And the manufacturer can, on a system-by-system basis, choose whether to populate a motherboard-resident connector with a flash-memory module for ReadyDrive use.

Turbo Memory and HyperFlash advocates also suggest that the system-side software for managing the flash memory and the hard drive and acting as arbiter between them is conceptually no different from today's already-mature software-RAID (redundant-array-of inexpensive-disks) utilities. And, as a Microsoft engineer pointed out to me at WinHEC, by virtue of the fact that they are both system-based, a Turbo Memory or a HyperFlash array could in the future cache not only the hard drive, but also other system-installed and network-connected storage peripherals, such as optical drives and NAS (network-attached storage, **Reference 5**). Regardless of the ReadyDrive array's location, it must, like a ReadyBoost subsystem, meet certain performance and other criteria to obtain Windows Vista Logo certification (**Table 1**).

"Microsoft recommends an NV cache size of at least 128 Mbytes to realize performance benefits for Windows Vista. To take advantage of the NV cache for the purposes of launching OEM-specified programs and to realize further performance benefits, an NV cache as large as 256 Mbytes to 1 Gbyte would be more effective. The larger the NV cache size, the more ReadyDrive can take advantage of the NV cache to deliver user benefits. However, NV cache sizes as small as 50 Mbytes are supported by ReadyDrive in Windows Vista. It is anticipated that future price reductions in the cost of flash memory and the increasing benefits from better performing flash technology will soon make NV cache sizes of 1 Gbyte or more practical and desirable. ReadyDrive can support NV cache sizes up to 2 Tbytes."

MAGNETIC: ANACHRONISTIC?

Instead of supplementing the hard drive with flash memory, you might instead choose to replace it with a solid-state drive. Suppliers such as Apacer, Mtron, PNY, PQI, Samsung, Sandisk (by virtue of its acquisition of M-Systems), STEC, Super Talent, and Transcend are vigorously promoting 1.8- to 3.5-in. solid-state drives as hard-disk-drive replacements for both general-purpose and embedded-computing applications. Vendors such as Bitmicro Networks and Texas Memory Systems focus on nearer-term solid-state-drive niches. And hard-disk-drive suppliers have already largely ceded the market for 1-in. and smaller form factors to solid-state-drive manufacturers.

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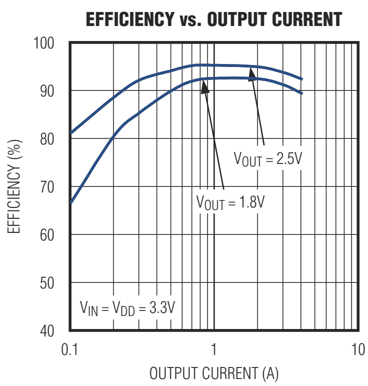

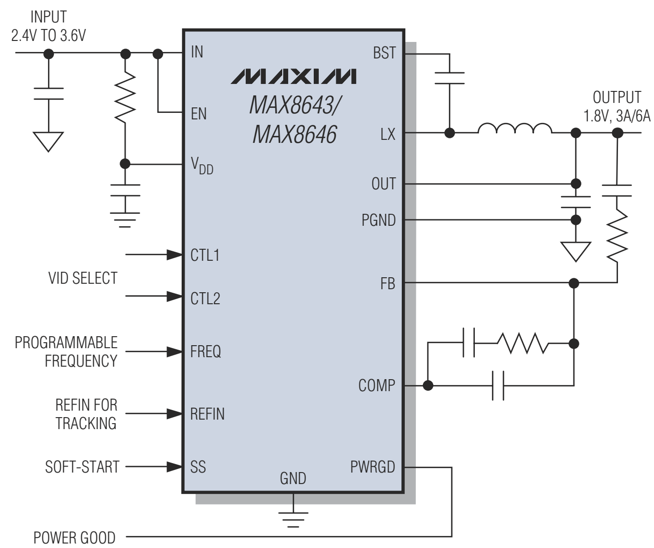

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You might ask: Aren't solid-state drives expensive? The answer depends on various factors. The solid-state drives' prices—at least to a first-order approximation—linearly scale with capacity, whereas hard-disk drives have a capacity-independent price "floor." The cost of the platters, chassis, pickup head, and other mechanical elements determines this floor price. Commensurate with that fact, the smallest hard-disk capacity, which each platter's per-side areal density determines, is on a seemingly constant upward climb, which the recent transition from longitudinal- to perpendicular-recording technology has further extended.

Therefore, if your storage needs are moderate and increasing at a slower rate than hard-drive capacities are growing, you'll eventually reach a point at which the constructed cost of a sufficiently dense solid-state drive will be less than the floor cost of a single-platter hard-disk drive. In non-PC applications, this hard-disk-drive-to-solid-state-drive transition has in many cases already occurred; one notable example is the obsolescence of Apple's 1-in.-hard-drive-based iPod mini after only 18 months of production and its replacement with the flash-memory-based iPod nano.

The Apple iPod case is equally useful in highlighting other advantages of a solid-state drive over a hard-disk drive. Highly mobile computing platforms, such as Windows Tablet PCs and UMPCs (ultramobile personal computers), and portable multimedia players value the inherent ruggedness of a solid-state drive. For example, mobile-computer supplier Alienware offers the m9750, m9700, and m5550 laptops, which optionally employ two 32-Gbyte solid-state drives in a RAID 0 striped arrangement. Asus, Dell, Fujitsu, Palm, Samsung, Sony, and Toshiba are also producing numerous solid-state-drive-based designs, despite these systems' substantial near-term price increment and capacity decrement over hard-drive alternatives. These manufacturers' decisions lead me to two encouraging conclusions: First, the vendors wholeheartedly buy into solid-state drives' inherent benefits. Second, they believe that industry participants will fairly quickly resolve solid-state-drive capacity and cost issues in target markets, therefore justifying today's market cultivation.

The lack of a motor-driven rotating platter may also provide these drives with lower average power and energy consumption, although hard-drive suppliers dispute this point. These objections are valid in some situations, such as when RAM- and flash-memory-caching techniques enable the hard drive to remain in spin-down for a large percentage of its operating interval and when other subsystems, such as a high-performance CPU and the LCD's backlight, also consume a notable portion of the battery's stored capacity.

Do you want other reasons to consider using a solid-state drive? Ponder, for example, Seagate's recent announcement that, by early 2008, it plans to no longer produce PATA (parallel-ATA)-interface hard drives, instead exclusively focusing its attention on SATA (serial-ATA) drives (**references 6** and **7**). Solid-state drives conversely come in a variety of interface and form-factor options, and you'll likely be able to continue purchasing them far into the future, given the suppliers' greater focus on non-PC applications. Consider, too, that moderate-sized flash-memory arrays take up less system-board surface area and overall system volume than a hard drive does. And don't forget about solid-state drives' potentially better performance than that of hard-disk drives. This superiority is unquestionably true with read accesses and also possibly true for writes, depending on the application's average data-set size and write frequency and how aggressively—at a power-consumption penalty—the solid-state-drive controller implements multiple parallel updates to multiple array components and multiple blocks with each component. According to Microsoft, you can now buy NAND-flash memory with faster sequential-data access and much faster random data access than mobile-PC hard drives offer. EDN

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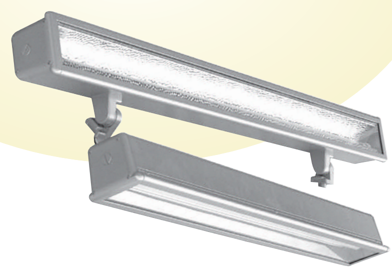

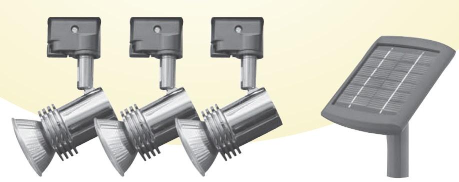


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Electronic systems have been major contributors to the success and popularity of all types of auto racing, from basic stock cars to the highly modified dragsters or Formula 1 machines that stretch the limits of engine and chassis design. As fans enjoy their favorite motor-sport competition at the track or on television, they see the culmination of years of research, data collection, and refinement that designers base on embedded-system technology. From prerace optimization to postrace analysis, auto-racing teams increasingly rely on mounds of engine and mechanical data to refine designs and increase performance. In the event of a crash, embedded recorders capture multiple data streams to identify mechanical failures or driver errors. But many of these electronic systems are controversial, and racing officials must continually update the rules to balance driver safety, fan enjoyment, and competitiveness.

Electronics in auto racing: FRIEND AND FOE

BY WARREN WEBB • TECHNICAL EDITOR

ALTHOUGH EMBEDDED-SYSTEM TECHNOLOGY IMPROVES ALMOST EVERY ASPECT OF MOTOR SPORTS, RACE OFFICIALS OFTEN BAN IT DURING COMPETITION IN THE INTEREST OF FAIRNESS.

Motor sports have inspired numerous embedded-electronics innovations that have eventually found their way into production automobiles. Embedded processors gather and exchange information to control, optimize, and monitor many of the functions that just a few years ago were purely mechanical. Power-train computers examine multiple sensors in real time and adjust fuel mixtures, ignition timing, and the transmission for the best performance. Designers base antilock-braking, traction-control, and stability-control systems on embedded electronics. In racing-specific applications, embedded systems can adjust the body configuration to improve aerodynamics and tune active suspension systems to a specific track. With real-time communications, pit crews can monitor and adjust engine performance, and fans get a view from the cockpit. Ironically, few motor-sport events allow many of the advanced electronic subsystems that racing teams have developed and refined. Officials may bar any subsystem that compensates for or assists driver actions in the interest of competition.

Individual sanctioning bodies, such as NASCAR (National Association for Stock Car Auto Racing), the Indy Racing League, or the FIA (Federation Internationale de l'Automobile), maintain rule books detailing the requirements for participation in racing events. NASCAR dates back to 1948 and claims to be the No. 1 spectator sport. It boasts 17 of the top 20 most-attended sporting events in the United States and is No. 2 in worldwide regular-season television

AT A GLANCE

- To ensure that race-car drivers—not clever computer programs—win races, competitions sometimes ban embedded electronics.
- Auto racing provides a test environment for high-performance vehicle- and safety-enhancement systems destined for production automobiles.
- In the event of a racing accident, event-data recorders capture the real-time sensor information to deliver immediate medical support.
- In the interest of fairness when employing embedded systems, some racing venues plan to supply racing teams with standardized engine-control units.

sports, with broadcasts in more than 150 countries. The FIA, which centers itself mainly in Europe but hosts events worldwide, sanctions Formula 1 or Grand Prix racing with highly customized cars designed for high-speed competition. Designers fully instrument most Formula 1 vehicles to deliver a real-time stream of car and driver information to the racing team, broadcasters, and spectators. The Indy Racing League is the governing body for another open-wheel, single-seat-style race car that the Indianapolis 500 features.

PRERACE OPTIMIZATION

Teams make many of the racing decisions and refinements long before the car ever touches the track. For example, Penske Technology Group works with motor-sport teams to predict vehicle performance before an event. Penske offers a computer-controlled shaker table along with analysis services it bases on software from The MathWorks to determine the best adjustments to vehicle-damping characteristics (**Figure 1**). The shaker rig provides seven hydraulic actuators, including four for road simulation and three that connect directly to the body of the car to simulate banking, cornering, and wind loads. Racing teams use prerecorded data from the track to tune vehicle dynamics by adjusting spring and shock parameters. Penske also uses The MathWorks' Simulink simulation tool to model aerodynamic loads that determine the proper download force for the actuators.

With vehicles traveling at more than 200 mph and only inches apart, auto-racing accidents are inevitable and frequent. However, only after the 2001 death of stock-car legend Dale Earnhardt did NASCAR begin collecting real-time crash data with an embedded-electronics event-data recorder from Independent Witness. NASCAR officials install the Witness—a self-contained unit with a two-year battery—next to the driver's seat. The device monitors vehicle motion and, in the event of impact, records the date, time, direction, impact, and severity, as well as a 3-D acceleration profile. Similarly, the Indy Racing League requires all cars to include the Delphi ADR3 accident-data recorder (**Figure 2**). The ADR3 can sense and record multiple vehicle parameters at 1k sample/sec before, during, and after an accident. Monitored parameters can include wheel speed, throttle position, steering angle, tire pressure, acceleration, and seat-belt loads. An ear-plug sensor that the driver wears contains embedded accelerometers that send G-force data immediately upon impact. On-site medical personnel can rapidly retrieve and analyze impact data to help them anticipate the types of injuries a driver may have suffered so they can prepare appropriate treatment. The data from multiple accidents has led to the integration of additional safety features into the cars, such as head and neck restraints to counteract impact forces.

In a move to adopt the benefits of embedded electronics and maintain fairness, the FIA has defined a standardized ECU (engine-control unit) for all Formula 1 racing teams starting in 2008.

Figure 1 Penske Technology Group offers racing teams a shaker table and software to determine the best adjustments to vehicle-damping characteristics.

Figure 2 The Delphi ADR3 can sense and record multiple vehicle parameters at 1k sample/sec before, during, and after an accident.

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Figure 3 The NASCAR PitCommand feature allows fans to track race-car position, speed, and engine rpm in real time on their computers (above).

Figure 4 RaceView provides fans with 3-D animation similar to that of sports video games to track their favorite drivers during racing events (right).

The ECUs will monitor all aspects of the power train and gather data from more than 100 sensors on each car while displaying critical information to the driver. Generating as much as 500 kbytes of data per second, a single ECU can potentially gather more than 1 Gbyte of information from the sensors during a Grand Prix race. A high-speed telemetry link continuously broadcasts this data back to systems in the pit-side garage of each Formula 1 team for detailed analysis. The FIA selected McLaren Electronic Systems and Microsoft as official suppliers of the standard Formula 1 ECUs and associated software.

TELEMETRY TROUBLES

By its nature, real-time telemetry data is also controversial in auto racing. With the proper setup, pit crews or even factory specialists can monitor vehicle sensors during the race to prepare for pit stops, devise alternative strategies for fuel conservation, or even identify and troubleshoot engine or mechanical malfunctions. Typical telemetry measurements include multiaxis acceleration, temperature, rotational speeds, and mechanical displacement. With two-way telemetry, experts can tune the engine performance or adjust aerodynamic characteristic in real time throughout a race. Sanctioning organizations now standardize the type and quantity of telemetry data allowed, and most ban two-way telemetry altogether.

One of the fastest growing segments in racing for embedded-electronic systems and software is in delivering real-time race information to the fans, either through television or over the Internet. Embedded-system designers working with broadcast teams and race officials have devised a number of concepts to capture and display real-time statistics. Most of these systems require precise position-location information for each car (see **sidebar** "Real-time tracking: Where's my car?"). NASCAR has been on the leading edge of subscription-based information systems that allow fans to closely follow the action with customized views of the race on the Internet. For example, the NASCAR PitCommand subscription service is an online Java-based multimedia feature that allows fans to track car position, speed, and engine rpm on their computers for any or all of the cars with real-

REAL-TIME TRACKING: WHERE'S MY CAR?

Combining high-speed data communications, global-positioning technology, and real-time camera control, the Racef/x system from Sportvision provides graphical enhancements for live television coverage of racing events. The system allows the announcer to activate on-screen pointers to identify selected cars in the race along with an optional virtual dashboard showing vital statistics, such as speed and position in real time. The system employs an onboard telemetry system to send sensor and GPS (global-positioning-system) data to a network of receivers in strategic positions around the track. Differential-GPS techniques determine each car's position, comparing satellite-position signals to known fixed positions. Several of the broadcast cameras include remotely controlled pan and tilt heads, enabling them to automatically follow the position data from the selected car. Updated several times per second, custom software synchronizes transmissions and collects statistics from as many as 55 cars racing around the track at more than 200 mph. Sportvision introduced its Racef/x system during the 2006 Indy Racing League season, and NASCAR (National Association for Stock Car Auto Racing) is now also using the system in its 2007 Busch series season. This type of tracking system also allows sanctioning organizations to capture additional revenue with subscription-based data it delivers over the Internet so that users can follow their favorite competitors.

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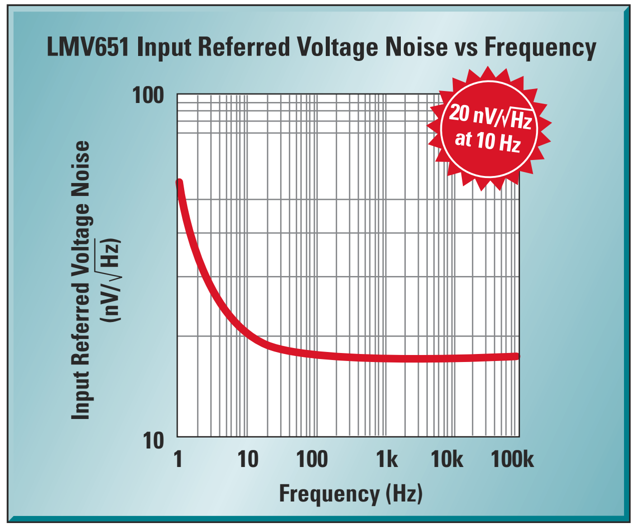

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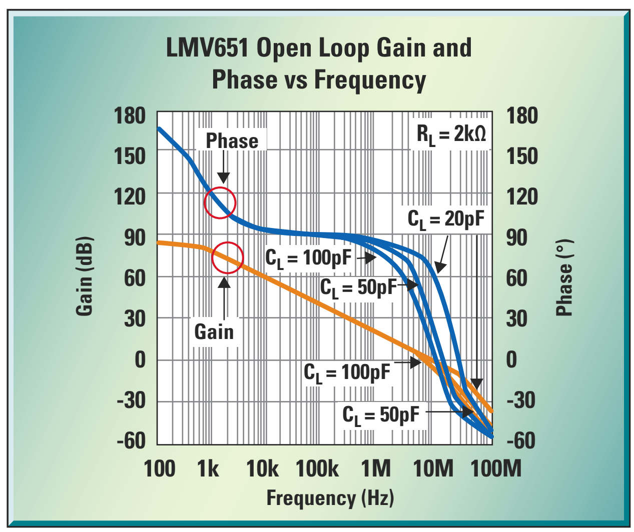

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Figure 5 The Boss Chevy Tahoe sport-utility vehicle from Carnegie Mellon University will compete in the driverless DARPA Urban Challenge.

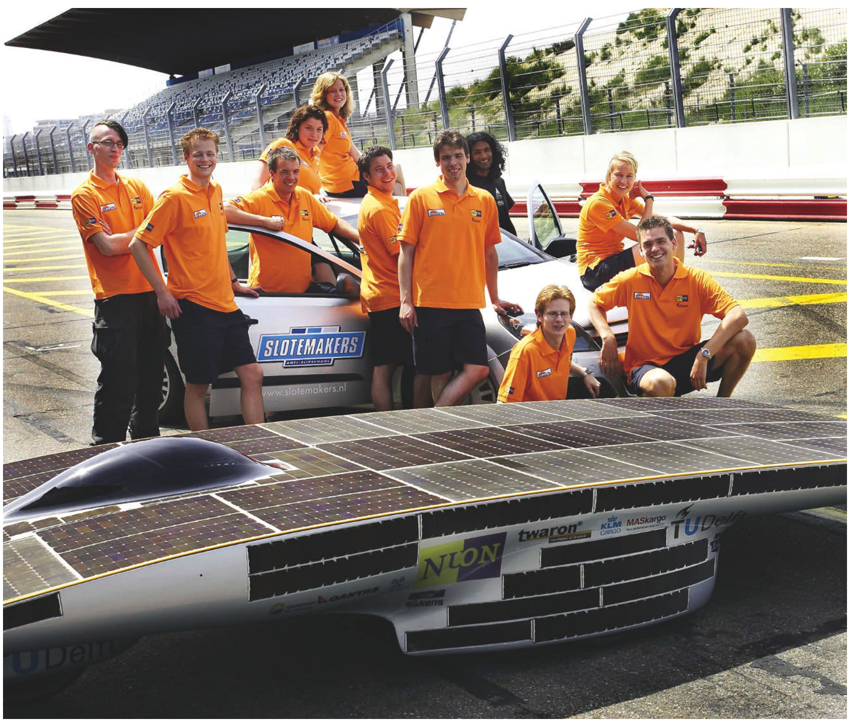

Figure 6 Only sunlight powered the Nuna3, which won the 3021-km World Solar Challenge in 2005 with an average speed of 103 km/hr.

time data directly from telemetry boxes in every car (**Figure 3**). RaceView, another NASCAR fan-data-delivery innovation, provides a computer application that features 3-D animation similar to that in popular sports video games (**Figure 4**). Fans can select one driver or switch among the full field of drivers to follow them around the track and during pit stops, caution flags, and lead changes and view driver data, such as live position, speed, and time behind the leader. Three race views are available for each driver, including Lead View, which shows the front of the driver's car, as well as the cars in pursuit; Flyover View, an aerial view from above; and Draft View, which shows the car from behind and the field in front of the driver. PitCommand and RaceView are part of NASCAR's premium subscription service for which fans pay a monthly fee of $12.95.

Although embedded-system technology may be controversial and some venues partially ban it, other races not only allow electronic systems, but also base results solely on their performance. For example, the top 20 teams from a qualifying event will compete in the DARPA (Defense Advanced Research Projects Agency) Urban Challenge in November for cash prizes worth $2 million for first place, $1 million for second, and $500,000 for third. Driverless robotic vehicles will conduct simulated supply missions on a network of urban roads at a military training facility in Victorville, CA. Vehicles must be entirely autonomous, using only a GPS (global-positioning system) and the information it detects with its sensors. In addition, vehicles must be stock or have a documented safety record and obey California driving laws. DARPA will provide the route network 24 hours before the race starts and provide each team a file detailing the route five minutes before the race starts.

ROBOTIC SUV

Tartan Racing of Carnegie Mellon University (Pittsburgh) is representative of the teams participating in the Urban Challenge. Its entry, named Boss, is a Chevy Tahoe sport-utility vehicle with more than 300,000 lines of code to autonomously navigate in town and in traffic (**Figure 5**). Boss uses perception, planning, and behavioral software to reason about traffic and take appropriate actions while proceeding to a destination. The vehicle includes more than a dozen lasers, cameras, and radars to view surroundings. Software and sensor technology allow the vehicle to detect and track other vehicles at long ranges, find a spot and park in a parking lot, obey in-

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⊞ For more on vehicle electronics, see "Black boxes capture car-crash data, controversy," www.edn.com/article/CA529380.

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tersection-precedence rules, follow vehicles at a safe distance, and react to dynamic conditions, such as blocked roads or broken-down vehicles.

The World Solar Challenge is another interesting racing event that depends heavily on embedded-electronic systems. The challenge is to design and build a car capable of crossing Australia using only sunlight as fuel. The winning car from the last race in 2005 covered the 3021 km between Darwin and Adelaide in 29 hours and 11 minutes, averaging about 103 km/hr. The car, Nuna3, relied on high-efficiency, three-layer, gallium-arsenide solar cells of a type normally used to power orbital satellites (**Figure 6**). Eleven students from different disciplines of the Delft University of Technology, Netherlands, designed and built the vehicle. The 2007 event, which will take place in October, will employ new rules to increase competition. Officials will restrict entrants to 6m^2 of solar collectors, driver access and egress must be unaided, and seating position must be upright. There are also many new safety requirements. Further, competitors will have to adhere to the new 130-km/hr speed limit across a portion of the course.

Although auto racing is not always ready for the latest in embedded electronics, it provides an excellent test bed for vehicle-performance and safety-enhancement systems. Designers have used embedded devices to improve the operation of vehicle power plants, transmissions, aerodynamics, fuel economy, and safety systems. Whether the competition tests speed at the track, reliability across the desert, or egos at the next stoplight, racing enthusiasts will continue to depend on electronics technology to keep ahead of the pack. **EDN**

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You can reach Technical Editor Warren Webb at 1-858-513-3713 and wwebb@edn.com.

BY HIREN SHAH • XP POWER

Designing small, efficient ac/dc switching power supplies

POWER SUPPLIES MUST PERFORM TO THEIR SPECIFICATIONS AS WELL AS MEET INTERNATIONAL STANDARDS WITH RESPECT TO EMC PERFORMANCE, SAFETY, AND INPUT PROTECTION. THESE TIPS INVOLVE SAVING SPACE WITHOUT COMPROMISING ELECTRICAL PERFORMANCE.

AC/DC-power-supply design is evolutionary, rather than revolutionary, developing largely as a result of gradual improvements in semiconductors and passive-component technologies and materials. Invariably, power-supply-design objectives involve not only meeting basic input and output specifications but also meeting them within a given package size and tight cost constraints. Some tried-and-true techniques, in a logical sequence from the input to the output of the power supply, can help you meet your goal.

The largest components in input filters are the inductors and capacitors. It pays to keep track of the latest products from all of the main toroid manufacturers, as sizes continue to shrink with developments in materials. With respect to Class X capacitors, which must operate across the mains line, you may be tempted to use ceramic types for their small size. However, these devices can fail catastrophically in the face of input spikes. Metallized polypropylene types, although larger, cope better with these spikes, as they have an inherent self-healing property. Self-healing removes a fault or short circuit by vaporizing the electrode in the region of the short and restoring the capacitor to useful life. Any loss of capacitance is negligible in normal operation. As with magnetic components, there will be gradual reductions in capacitor size over time.

To meet safety requirements with respect to creepage and clearance, you must leave a physical-safety margin at the edges of bobbins for winding inductors and transformers. A triple-insulated, UL-certified, copper wire can remove the need for these gaps; you can then wind right to the edge of the bobbin. With this process, you can reduce the overall size of the switching transformer, often the largest component on the board, by as much as 20%.

Carefully select the working voltage of aluminum-electrolytic capacitors to get the best combination of minimum size and extended operating life. These capacitors have longer operational life when you use them at no more than 80% of their rated voltage. If you use the capacitors at full rated volt-

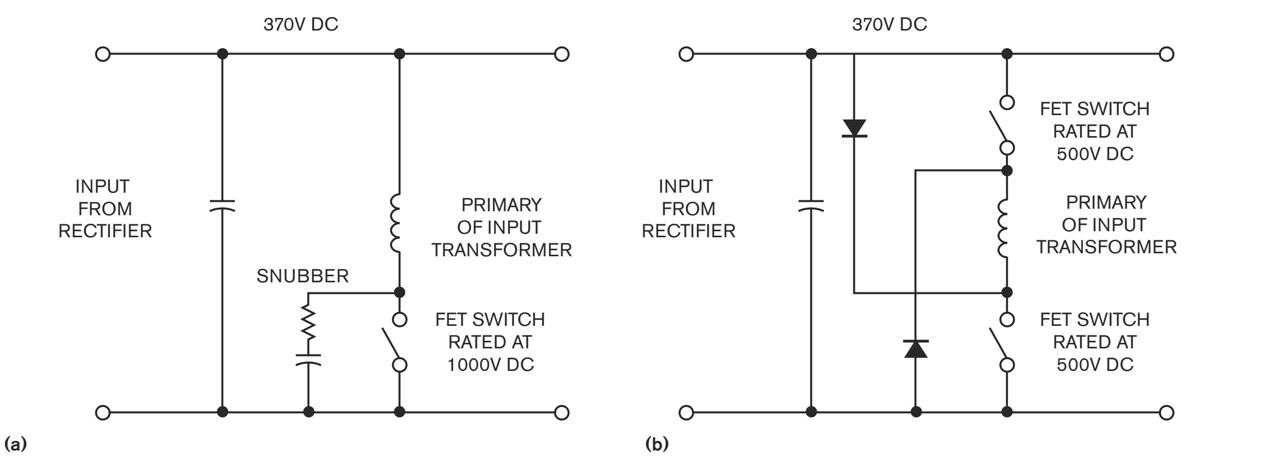

Figure 1 Although it minimizes component count, a single 1000V FET switch (a) is more expensive and less efficient than a circuit with dual 500V FET switches (b).

age, leakage current produces heating losses that can degrade the components. The rule of thumb is that every 10°C increase in temperature halves the life of the capacitor. In practice, the dielectric layer in the capacitors will reform to the voltage at which you are using them, and any voltage surge can result in circuit failure, so the design should take this information into account, too. Use components with a 105°C temperature specification for the longest operating life. In practice, a relatively large capacitor will be necessary anyway, not just for ripple reduction but to provide the required dc holdup time in the event of short-term disruption in the ac input. Typically, a holdup time of 10 to 20 msec is necessary. Large electrolytics have high ESR (equivalent series resistance) at higher frequencies, so it's always good practice to include a much smaller capacitor—often a plastic-film type, around 0.22 μF—in parallel to reduce this value.

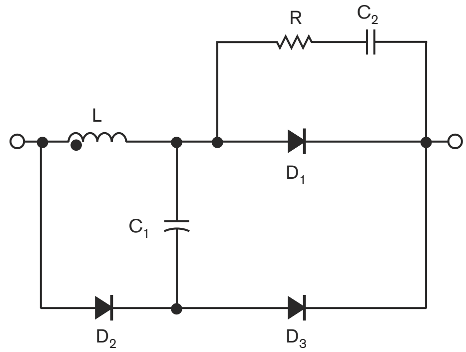

Figure 2 The snubber circuit you need with conventional diodes adds cost and complexity.

Designers base most of their products on a dc input to the switch of 370V, based on 1.4 times the high-line ac voltage of 264V. If you use a single MOSFET for switching, having the back EMF that the stored energy in the input-transformer primary generates when the switch opens will mean that you have to use a 1000V-dc-rated MOSFET. These devices are available but relatively expensive. They also have high forward resistance (R_{DSON}) that may reach 40 mΩ, compromising efficiency. You also need to include a snubber circuit to prevent high voltage spikes from damaging the MOSFET and to add reset winding in the main transformer and other components, increasing component count, cost, and board space. A smarter approach is to use two 500V MOSFET switches (S_1 and S_2) as in **Figure 1**. The switches operate simultaneously on either side of the transformer secondary, and the diodes conduct at approximately 1V above the input voltage, clamping the maximum voltage that back EMF creates, protecting the input capacitor, and eliminating the need for a snubber circuit. Costs for 500V MOSFET switches are approximately one-sixth that of 1000V-rated versions, and a number of vendors now offer devices with forward resistance as low as 5 mΩ.

Figure 3 The compact MFA350 350W ac/dc switching power supply from XP Power achieves 11.2W-per-cubic-inch power density.

SiC (silicon-carbide) rectifiers in boost converters may appear to be expensive, but when you calculate the reduction in component count that's possible, the reduced power-supply assembly cost, and the savings in board space, you'll probably find that an overall cost disadvantage no longer exists. What's more, their use can deliver a 1% improvement in total power-supply efficiency. Conventional diodes permit high reverse current, and the design needs to dissipate the energy in a snubber circuit comprising two diodes, two capacitors, a resistor, and an inductor (**Figure 2**). The negligible reverse current of the SiC diode eliminates these six components and reduces losses, leading to improved efficiency. Both Cree (www.cree.com) and Infineon (www.infineon.com) offer SiC diodes.

It's now also economical to combine through-hole and surface-mount techniques in the design of ac/dc switchers. You can implement control functions on the underside of the pc board using surface-mounted devices.

Where possible, affix power semiconductors directly to the power-supply case or U-channel. You no longer need thermal pastes. Thermal-transfer components from companies such as Bergquist (www.bergquistcompany.com) allow you to solder the tabs of power devices directly to a copper pad that is already bonded to an electrically insulating but thermally conductive substrate. This approach is inherently more consistent and reliable than using thermal pastes. Where you need forced-air cooling, you might consider three-wire intelligent fans. The fan speed varies with temperature to ensure that the fan runs only as fast as it needs to for given operating conditions, reducing both noise and power consumption. However, the relatively high prices of these fans and the ready availability of low-cost fan-control chips make implementing your own control circuit more cost-effective. Fan noise is another consideration. Experiment with the format and spacing of finger guards. Placing finger guards a few millimeters away from the panel on which the fan is mounted, rather than flush with it, can reduce fan noise by 5 to 6 dB. In a system that uses a number of power supplies, this reduction is audible.

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Don't let all the hype about digital control for ac/dc power supplies carry you away, unless your application absolutely needs it. Designers have widely implemented digital control in point-of-load converters, but doing so adds considerable cost to ac/dc power supplies. The chips may now be available at 50 cents or so, but when you consider the additional components necessary, manufacturing costs, and the cost of connectors, implementing digital control will add $10 to $15 to the cost of an ac/dc power supply. This figure may be acceptable for a 1-kW power supply, where it is a small proportion of the total cost, but for low- to medium-power units, the additional cost is rarely justifiable.

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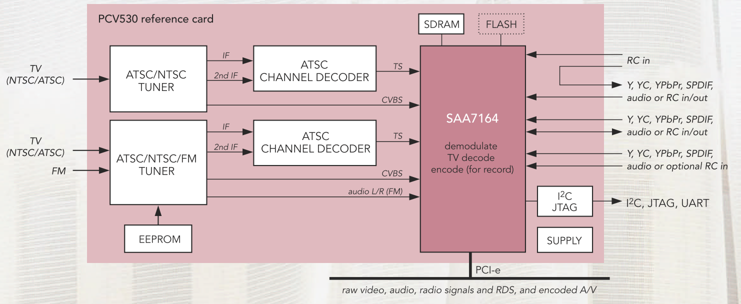
There is always room for creativity in mechanical design. Consider the range of applications for which you may use the power supply at the outset. For example, it may be possible to design the overall physical dimensions so that the power supply fits horizontally or vertically into an industry-standard enclosure format (**Figure 3**). You can design the pc board to accept plug-in connectors or screw terminals, adding no cost but greatly improving the application flexibility. And remember the small things, such as accessibility of fuses and reversible cable-retention devices, so that the walls of the system enclosure or other protuberances don't obstruct them. Stacking components to save PCB (printed-circuit-board) space is another technique that designers often overlook. For example, it may be possible to stack the inductors in a filter network on top of capacitors, simply fixing them with adhesive. This approach can also help EMC performance by keeping filter component interconnects very short.

To look at some power supplies, you might think that someone dropped the components onto the board from a great height and then connected them! Careful component layout that follows a logical flow from input to output is good engineering practice. The product looks better, is easier to test and service, and performs better. Remember, every bend in a PCB track adds a little inductance that can create electromagnetic interference. **EDN**

AUTHOR'S BIOGRAPHY

Hiren Shah is responsible for new-product development in the United States for XP Power, including managing the design team, working with sales and marketing to identify customer and market ideas for new products, and ensuring that the company launches its products on time. He received a BSEE from MS University of Baroda, India, in 1981 and has been with XP Power for 12 years. His interests include hiking, reading, and travel.



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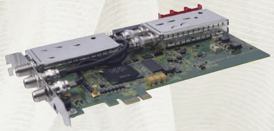

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Transforming motion: field-oriented control of ac motors

FOC PRINCIPLES SIMPLIFY THE ANALYSIS OF AC MACHINES AND ALLOW GOOD DYNAMIC CONTROL OF THE MACHINE FLUX AND TORQUE.

Once the control method of choice only in high-performance industrial ac-servo drives, FOC (field-oriented control) is finding its way into lower end industrial and many appliance applications with the advent of integrated FOC implementations.

Various electrical machines share common operating principles that a simple example can illustrate (**Figure 1a**). In this mechanism, the field winding produces a magnetic field in the air gap that interacts with the current-carrying coil on the armature. The first operating principle is that the electromagnetic force on the armature coil due to the magnetic field produces a torque proportional to the coil current. The second principle is that moving the coil in the magnetic field generates a voltage, known as back EMF (electromotive force), proportional to the angular velocity. When the coil rotates, the leading conductor continuously moves between poles of opposite polarity. Switching the polarity of current in the coil as it switches its alignment with the magnetic poles maintains unidirectional torque. The back EMF in the armature coil also switches polarity as it rotates. Thus, in an ideal machine, electrical energy continuously flows into the coil, equaling the continuous mechanical-energy output.

In the idealized form of this electric machine, a mechanical commutator switches the polarity of the coil connection to the brushes so that there are time-varying-dc currents and voltages (**Figure 1b**). This ideal dc electrical machine is a core element in the models of real dc and ac machines that control-system developers use. The following **equations** define machine torque (T), back EMF (e_A), and pole flux (ϕ) in terms of the armature current (i_A), the rotor's angular velocity (ω), and an armature constant (k_A) that accounts for the number of coil turns and the number of magnet-pole pairs: $T=k_A\phi_P i_A$, and $e_A=k_A\phi_P\omega$. Combining these **equations** results in $T\omega=k_A\phi_P i_A\omega=e_A i_A$, which shows that the system satisfies conservation of energy. The pole flux is a function of the field current (i_F) in a wound-field machine, $\phi=F(i_F)L\approx L_M i_F$, but is a constant in motors that use permanent magnets to generate the field, $\phi=\phi_M$.

In the dc machine, the magnetic-field system is fixed, and the current-carrying coils on the armature rotate. The real dc-machine model includes the winding inductance and resistance (**Figure 2**). If the voltage drop across the armature-winding resistance is relatively small, then the motor's back EMF will closely track the input dc voltage. A controller that increases the motor armature voltage as a function of the target speed can achieve open-loop speed control of the dc machine.

An alternative speed-control approach reduces the field-winding current and keeps the armature voltage constant. In

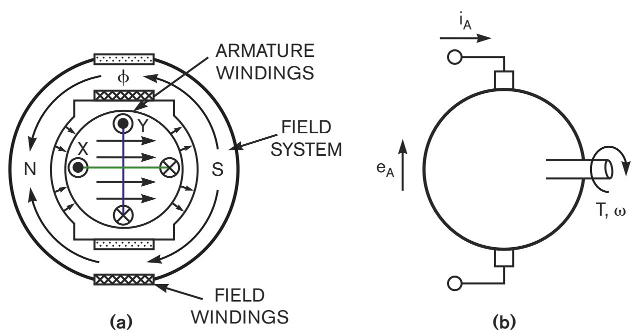

Figure 1 A model of an idealized electric machine relates armature current, back EMF, torque, and angular velocity (a). In an idealized form, a mechanical commutator switches the polarity of the coil connection to the brushes (b).

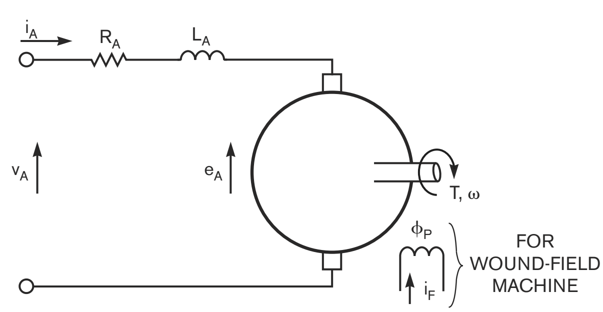

Figure 2 The dc machine's circuit model includes series resistance and inductance—both of which are parametric in temperature—that determine the winding's natural dynamic electrical response.

this case, the speed is inversely proportional to the pole flux, and the controller uses less current. Industrial-control-system designers prefer armature-voltage control because the speed is a linear function of the input voltage. However, field-voltage control allows the motor to further increase its speed after reaching the limit of its armature-supply voltage.

Closed-loop control provides a good dynamic response—a requirement in control systems for industrial robots and assembly equipment. The closed-loop control system typically has an inner current loop that compensates for the motor winding's natural dynamic response and an outer velocity loop that compensates for the mechanical system's dynamics. Typical designs set the current loop's bandwidth an order of magnitude wider than the velocity loop's bandwidth so that the dynamic response of the current loop does not affect the velocity loop's gain over its band of interest.

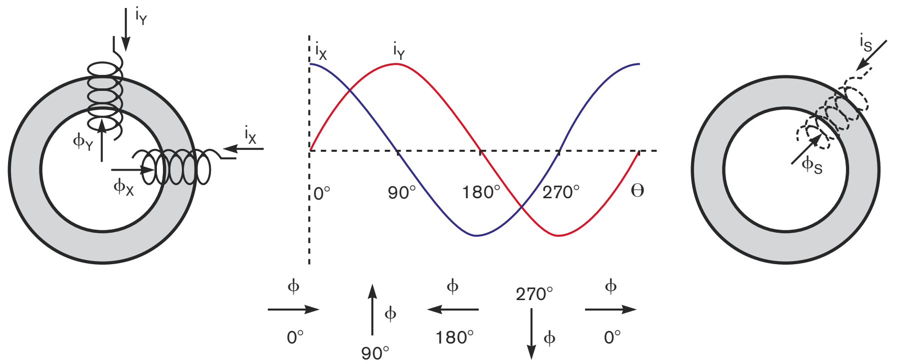

Figure 3 Direct- and quadrature-drive terms drive the two-phase ac machine with the equivalent of a rotating field.

A dc machine has a stationary field coil that controls the air-gap flux and rotating armature windings that carry the torque-producing currents. An ac machine has rotating field coils and stationary stator windings that generate torque. In either case, alignment of the current with the air-gap flux is necessary to produce a constant torque. In the ac machine, synchronization of the stator-frequency current with that of the rotor achieves this alignment. In the dc machine, the action of the brushes and commutator aligns the armature current with the stationary field system.

Considering the ac machine from a reference frame synchronized with the rotor makes the field system appear stationary. The stator windings appear as rotating-armature-type coils, and you can imagine a commutator system that switches the polarity of the current in these coils as they rotate. This principle is the basis of FOC, which models ac machines using equivalent dc machines with the aid of coordinate transformations. The dc models simplify the machine analysis by transforming ac currents and voltages that vary in both magnitude and frequency into dc currents and voltages.

MODELING AC MACHINES

In the simple machine of **Figure 1a**, the direct axis is the axis aligned with the field system, and the quadrature axis is normal to this axis. The machine produces maximum torque by aligning the armature coil with the quadrature axis. The two-phase ac machine contains a fixed-field system on the rotor, but magnetic flux coupled with the stator windings varies with the spinning rotor, so these windings generate ac voltages (**Figure 3**).

The spatial separation of the windings imposes a time delay between the flux waveforms coupled with each winding. The converse is also true, and driving time-phase-separated ac currents into spatially separated ac windings can generate a field system that appears to rotate at the frequency of the ac

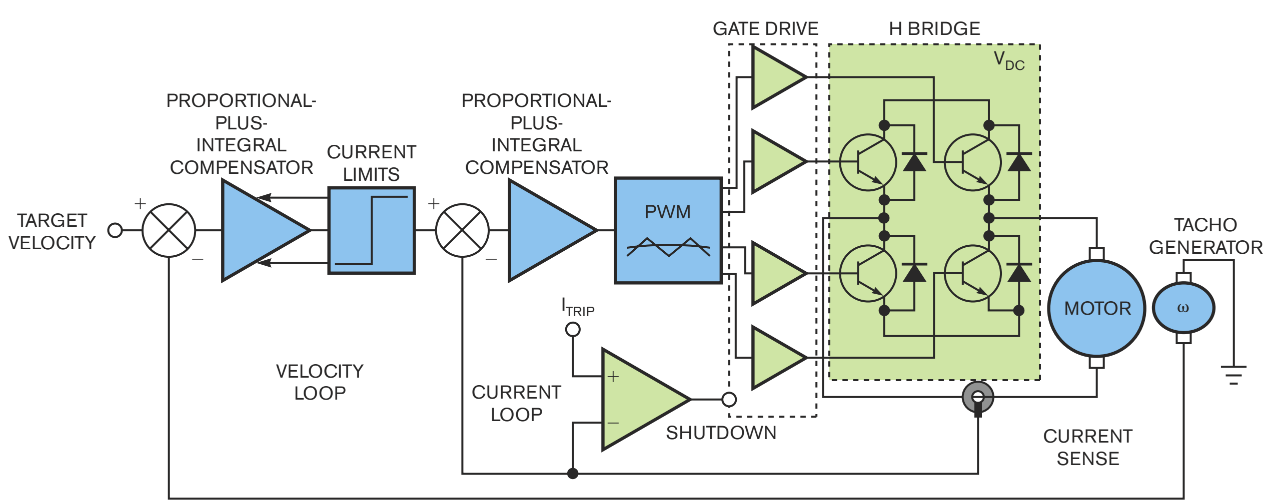

Figure 4 The dc-servo-control system comprises an inner current-control loop and an outer velocity-control loop.

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currents. The current in the Phase A winding acts along the X axis, and the Phase B winding acts along the Y axis. The ac currents in the winding are out-of-phase in time by 90°, so that the peak of the Phase A current occurs when the Phase B current is zero and vice versa. At the 0° electrical point, when the Phase A current is at its peak, the net field acts along the positive X axis. After a quarter of a cycle in time, Phase B is at its peak, and the net field acts along the Y axis. After a further quarter-cycle in time, the field acts along the negative X axis. In one electrical cycle of the ac-winding currents, the field rotates through a full 360°. Thus, the stationary two-phase windings with ac currents produce the same effect as a rotating winding with dc currents.

Several mathematical transforms help simplify modeling ac machines by transforming circuit descriptions between fixed- and rotating-reference frames. The forward-Park transform is a simple vector-rotation function that calculates the stator-winding flux as a function of the rotor flux and the rotor angle. It is a mapping between the rotating-reference frame of the rotor and the stationary-reference frame of the stator.

The reverse-Park transform calculates the equivalent rotating rotor-flux vectors corresponding to the stator-winding flux. This computation transforms the two-phase ac-machine currents and voltages in the two-phase ac machine's stator windings into an equivalent set of currents and voltages in rotating windings. The current values that the transform provides have two components: one directly aligned with the rotor flux (I_D) and another in quadrature with the rotor flux (I_Q). The direct component is equivalent to field-winding current, and the quadrature component is equivalent to dc-armature current. The transform simplifies the analysis of the two-phase ac machine by providing an analytic link in an equivalent dc model. This principle easily extends to the Clarke transform for three-phase machines by resolving the flux for each winding into components along the X and Y axes, which are necessary to calculate the two-phase-machine equivalent values.

FOC OF AC MACHINES

Electric-machine-design engineers many years ago developed the Park and Clarke transforms to simpifly ac-machine modeling. In modern applications, these transforms help improve ac-machine-controller designs. The basic principles in ac-machine control are that the stator-voltage magnitude must increase with frequency and the rotor speed must track this frequency. An open-loop control system uses a three-phase power inverter to vary the motor-winding voltages using a constant volt-per-hertz control law. However, this type of control does not deliver good dynamic control or maximize efficiency. Good dynamic control is possible using dc motors by controlling the armature current. In the dc-servo system, the outer loop calculates the torque necessary to correct the velocity error, and the inner loop adjusts the voltage to drive the current necessary to produce the desired torque (**Figure 4**). The control-loop tuning compensates for the armature-winding inductance and resistance.

The application of Clarke and reverse-Park transforms to stator-current values calculates the equivalent torque- and flux-current components in the rotating-reference frame. The transformed ac model now behaves like a wound-field dc machine. The ac-machine controller independently controls the torque and flux current by adjusting the rotating-reference-frame voltages V_D and V_Q (**Figure 5**).

The space-vector pulse-width modulator accepts the two-phase ac-reference inputs and calculates the three-phase inverter's timing signals. A major advantage of this control

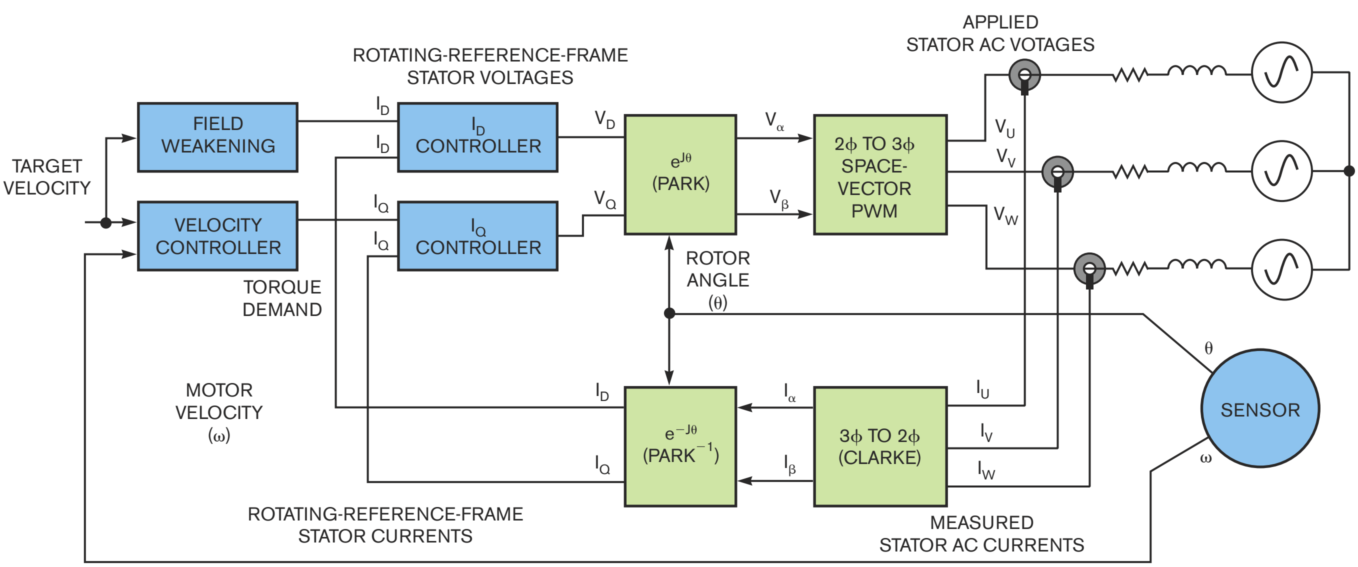

Figure 5 An FOC system for an ac machine transforms three-phase stator-current measurements and stator-drive voltages between rotating- and stationary-reference frames to simplify the control structure.

structure is that the current-loop compensation is independent of the stator frequency. The velocity-control loop performs the same function as it does in the dc-servo system and provides the input reference to the I_Q current loop that controls torque. The flux-control loop maintains a constant flux at low speeds to maximize efficiency but reduces flux at higher speeds in a field-control mode when the stator voltage reaches its limit.

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In a permanent-magnet ac machine, the controller sets the I_D-current reference to zero at low speeds because the rotor magnet produces all the flux. An induction motor requires magnetization current, so the controller sets I_D to maintain the rated flux in the low-speed range. Permanent-magnet ac machines operate with greater efficiency than induction machines at low speeds because they require no magnetization current. The converse is true in the high-speed range, because permanent-magnet ac machines require I_D-current injection to weaken the field to operate above the base speed.

A key variable in the application of FOC is the angle of the rotor flux. In the case of a permanent-magnet ac machine, the rotor flux aligns directly with the rotor. An ac-servo drive uses resolvers or absolute encoders to measure the rotor's angular position. The situation is more complex in ac-induction machines, because the rotor currents flow at the slip frequency and are inaccessible.

An accurate machine model combined with rotor-speed measurement enables flux estimation, but the rotor resistance varies significantly with frequency and temperature and is difficult to track (**Reference 1**). The slow reaction of the rotor circuit makes it difficult to achieve good dynamic performance. The permanent-magnet ac motor is preferable in most high-performance industrial drives because of its superior dynamic performance. However, a number of spindle drives use induction motors because of their superior performance in the high-speed field-weakening range.

In appliance and low-end industrial applications, a direct measurement of the rotor position is cost-prohibitive. However, the dramatic reduction during the past several years in the cost of computation has made economical a sensorless measurement of rotor position based on machine models. The two-phase circuit model of a permanent-magnet ac machine includes sine and cosine functions for the rotor flux. The Clarke transform calculates the two-phase-current values from three-phase motor-current measurements. The two-phase voltage values are outputs from the current control loops.

$$v_\alpha = R_S I_\alpha + L_S \frac{dI_\alpha}{dt} + \frac{d}{dt}(-\Psi_R \cos(\theta_R));$$

$$v_\beta = R_S I_\beta + L_S \frac{dI_\beta}{dt} + \frac{d}{dt}(-\Psi_R \sin(\theta_R)).$$

A simple reordering of the **equation** terms and mathematical integration yield the sine and cosine terms. Both angle and velocity data derive from a phase-locked-loop-tracking algorithm, similar to the type that resolver-to-digital-conversion ICs use (**Reference 2**):

$$\Psi_R \cos(\theta_R) = \int (R_S I_\alpha - v_\alpha) + L_S I_\alpha;$$

$$\Psi_R \sin(\theta_R) = \int (R_S I_\beta - v_\beta) + L_S I_\beta.$$

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AUTHOR'S BIOGRAPHY

Aengus Murray, PhD, a recognized expert in motor-control systems, joined International Rectifier in 2005. He is part of the leadership team furthering the company's product-marketing and -development efforts in energy-saving motor control and its flagship integrated design platform, iMotion. Murray received a bachelor's degree in electrical engineering and a doctorate in motor control from University College Dublin. Murray began his career with Kollmorgen Industrial Drives in Ireland and later joined Dublin City University, where he taught graduate and undergraduate courses in power electronics. He went on to spend 11 years with Analog Devices (Boston), where he led the company's motor-control-systems-engineering team.

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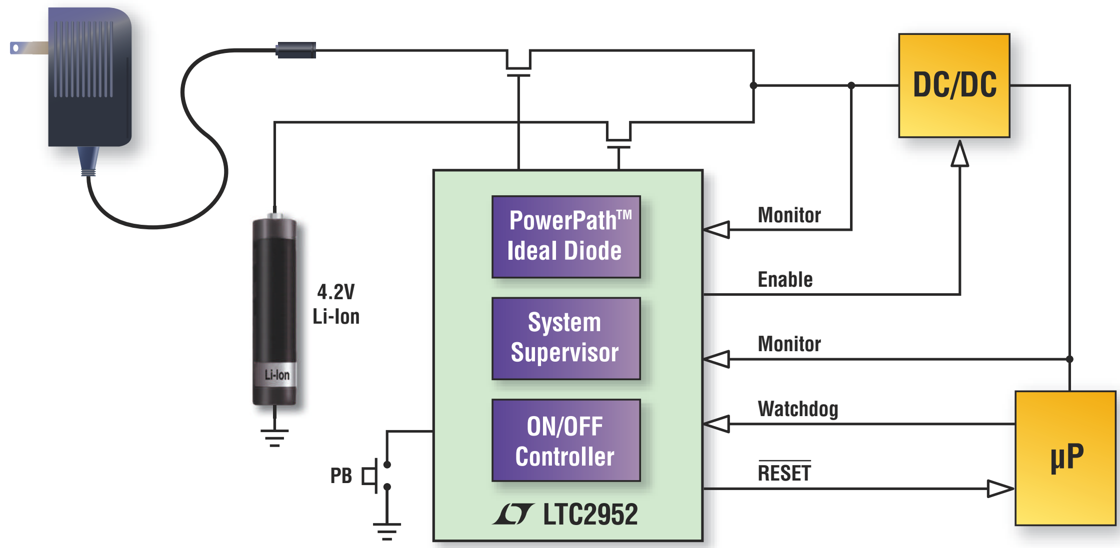

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LTC2952	2.7 to 28	25µA	Adj	Adj	Extendable	Push button power path controller with system monitoring	TSSOP-20, QFN-20
LTC2954	2.7 to 26	6µA	Adj	Adj		Interrupt logic for menu driven applications. Active high enable output (LTC2954-1), active low enable output (LTC2954-2)	TSOT-8, DFN-8

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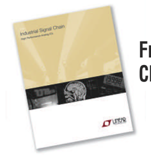

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LINEAR TECHNOLOGY

Single op amp achieves double-hysteresis-transfer characteristic

Herminio Martínez, Encarna García, and Juan Gámiz,
Technical University of Catalonia, Barcelona, Spain

In process-control applications requiring discontinuous controllers, the most elementary choice is a two-position-mode or on/off controller. A typical example of such a controller is a space heater. If the temperature drops below a setpoint, the heater turns on, and, if the temperature rises above the setpoint, it turns off. In the analog domain, the basis for the basic implementation of a two-position controller is an analog comparator or an open-loop operational amplifier. However, to avoid false switching, the typical implementation uses the well-known Schmitt trigger.

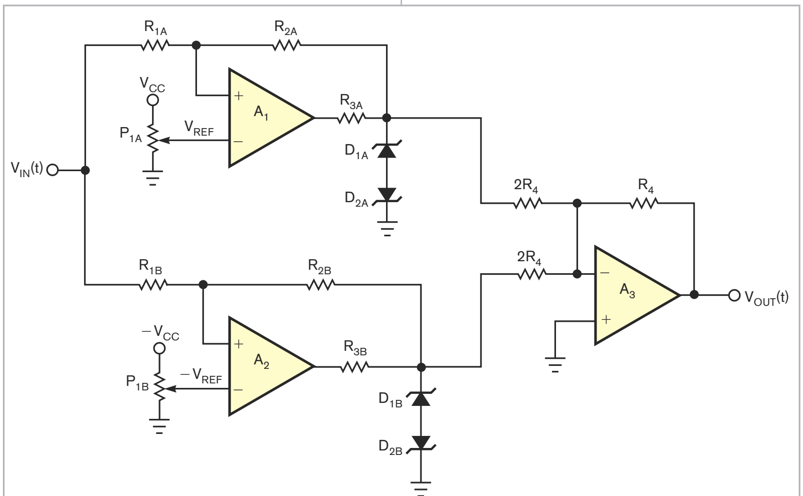

Figure 1 One straightforward way of obtaining a double-hysteresis-transfer characteristic uses three op amps with voltage references and zener diodes.

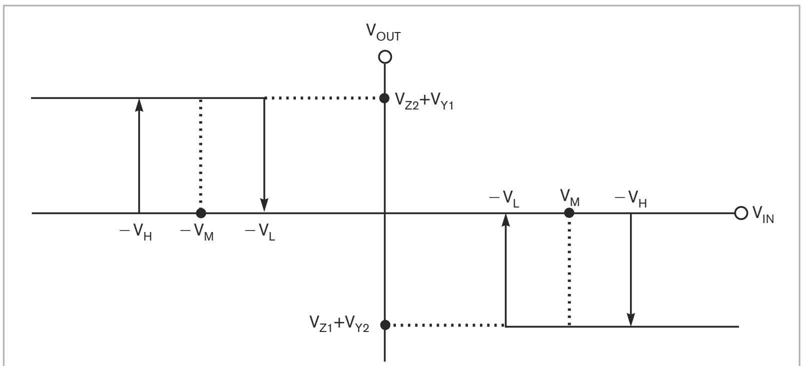

Figure 2 The I/O-transfer characteristic of the circuit in Figure1 exhibits two hysteresis bands.

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A logical extension of the two-position control mode is to provide several—rather than two—intermediate settings of the controller's output. You can use this discontinuous-control mode to reduce the cycling behavior, overshoot, or undershoot inherent in the two-position mode. In fact, however, it is usually speedier to use some other mode when the two-position mode is unsatisfactory. The most common example is the three-position controller. **Figure 1** shows one simple way to implement this controller. In this configuration, the Schmitt triggers around the operational amplifiers, A_1 and A_2, which implement the negative and positive hysteresis, respectively. You can replace A_1 and A_2 with analog comparators, such as an LM311 or similar. **Figure 2** shows the I/O-transfer characteristic of the circuit in **Figure 1**:

$$V_M = V_{REF}\frac{R_1+R_2}{R_2},$$

$$V_H = V_M + (V_Z + V_Y)\frac{R_1}{R_2},$$

and

$$V_L = V_M - (V_Z + V_Y)\frac{R_1}{R_2}.$$

V_Z and V_Y are, respectively, the breakdown and the forward voltages of the four zener diodes.

Figure 3 shows a more efficient way to implement a three-position controller. The circuit's basis is a single operational amplifier, and it needs no reference voltages. The input and output diodes determine the upper high-voltage and lower low-voltage switching-threshold levels and the hysteresis of the comparator. Putting $V_{IN}(t)$ in the middle band eliminates the input diodes from the circuit, and the circuit is essentially a voltage follower with positive feedback. The output voltage follows $V_A(t)$, but the positive feedback establishing $V_A(t)$ sets this voltage at some fraction of the output voltage. So, two constraints define the output level in this circuit state: $V_{OUT}(t)=V_A(t)$, and

$$V_A(t) = V_{OUT}(t)\frac{R_1}{R_1+R_2}.$$

The only condition satisfying these two constraints is that V_{OUT} and V_A=0V; so, the output remains at 0V when the input diodes are reverse-biased. A 0V output state continues until input voltage increases with positive or negative values. Then, one of the two input zener diodes conducts, driving the amplifier output positive or negative at an input voltage of $\pm V_H$. In this condition, when absolute input voltage decreases, the amplifier output again goes to 0V at an input voltage of $\pm V_L$. Thus, the design equations for V_H and V_L are $V_H=V_{Z1}+V_Y$, and

Figure 4 shows the I/O-transfer characteristic of the circuit with the values in **Figure 3**, where D_{1A} and D_{1B}

$$V_L = (V_{Z1} + V_{Y1}) - (V_{Z2} + V_{Y2})\frac{R_1}{R_1+R_2}.$$

are 6.8V 1N4099 zener diodes and D_{2A} and D_{2B} are 3V 1N5225 zener diodes. **Figure 5** shows the output voltage when you apply a triangular waveform at the circuit's input. **EDN**

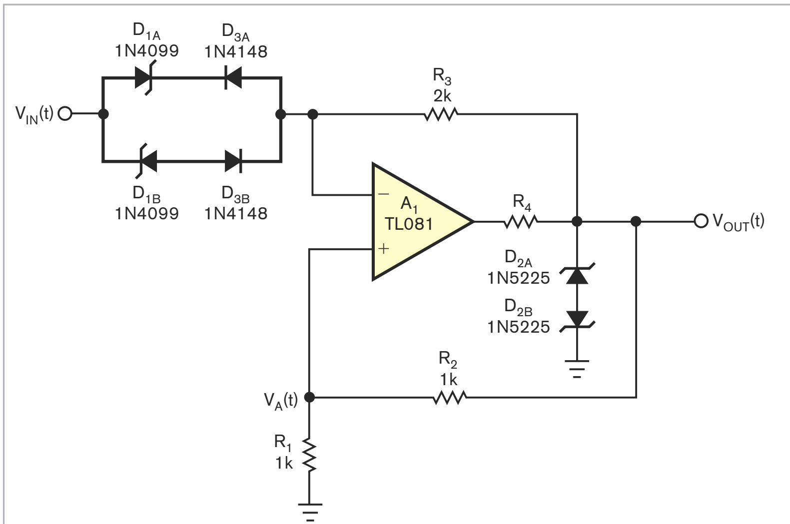

Figure 3 This circuit achieves dual hysteresis using only one op amp.

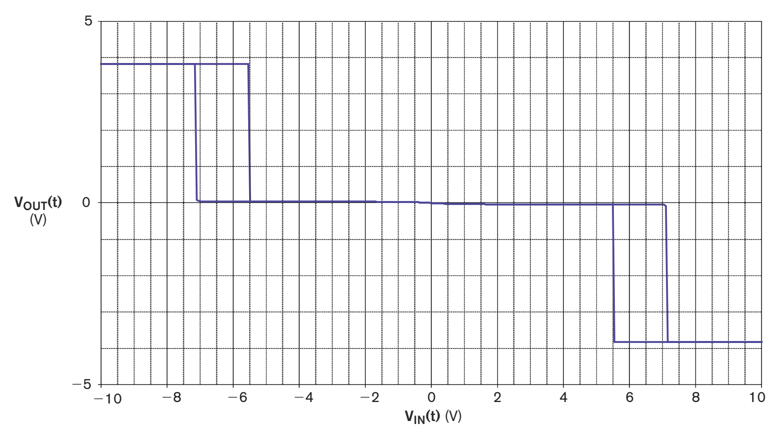

Figure 4 This oscilloscope trace shows the transfer characteristic of the circuit in Figure 3.

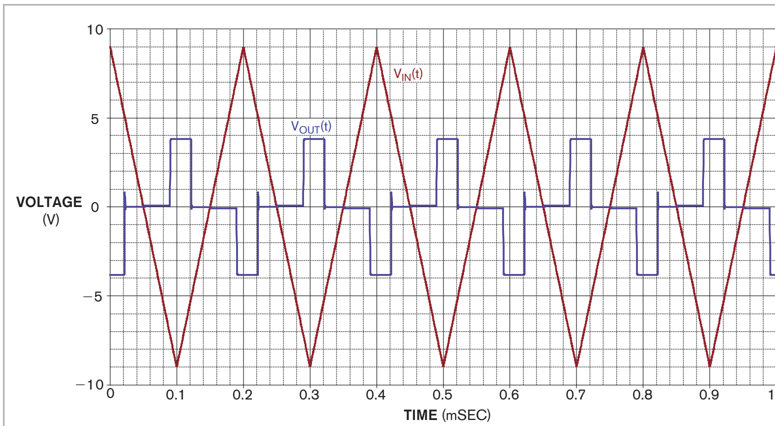

Figure 5 This oscilloscope trace shows the response of the circuit in Figure 3 to a triangular input waveform.

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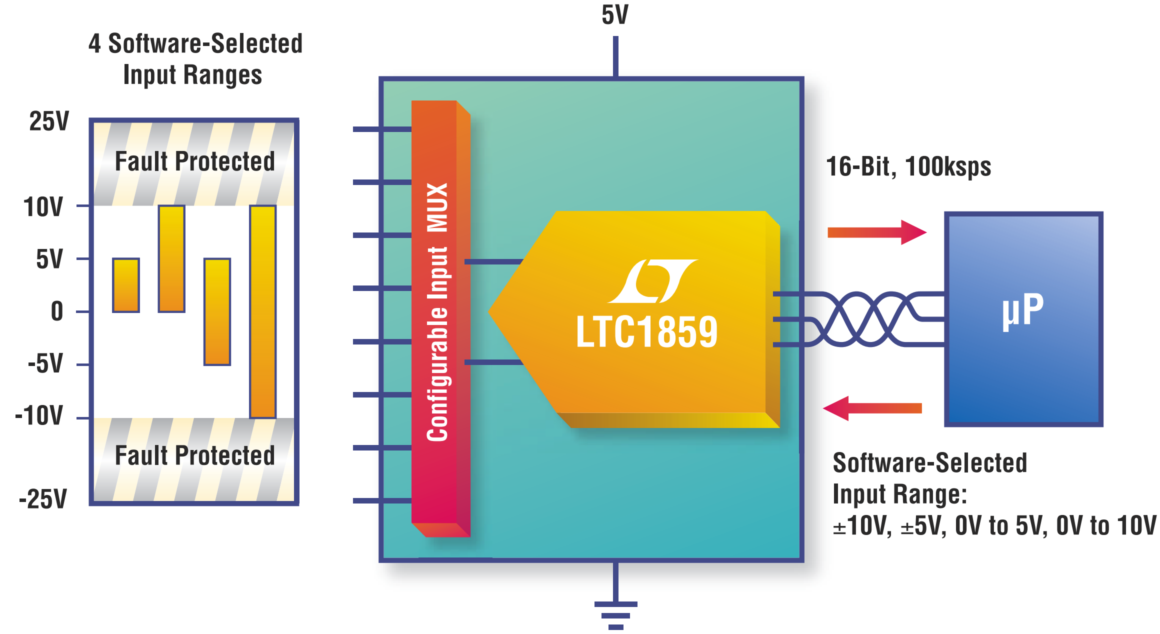

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LINEAR TECHNOLOGY

Integrator ramps up/down, holds output level

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

Op-amp integrators can ramp to saturation, and a capacitor-discharge switch can reset them. Alternatively, you can input-switch them to ramp up and down in triangle-waveform-generator applications. Much searching through online "cookbook" circuits turned up no means of ramping an op-amp integrator to hold at a preset constant voltage level. This Design Idea describes a single-supply op-amp circuit that outputs a rising or falling linear-voltage ramp in response to a step change of a positive dc-input voltage of 0V to V_{CC}. The output ramp's dV/dt slope is adjustable to 1V/minute with the values in **Figure 1**, is independent of the input-step amplitude, and terminates at a constant dc level approximately equal to the input-step voltage. Any further change in the dc-input voltage causes the output to ramp up or down at the preset dV/dt to the new dc-input voltage. In effect, this circuit is an amplitude-bounded constant-slope integrator.

The circuit uses a rail-to-rail I/O quad op amp, the National Semiconductor (www.national.com) LMC6484. The rail-to-rail feature makes it easy to use, the low input leakage is great for long-time-constant integration, and the 3-mV maximum input-offset voltage is respectable. Potentiometer R_1, a linear taper, sets the input voltage for final output voltage after the ramp ends. IC_{1A}'s output is in saturation at V_{CC} or ground while the output is ramping down or up, respectively.

Nonpolarized capacitor C_1 and potentiometer R_2, a linear taper, determine the time constant of integrator IC_{1B}. The adjustment range is 0.5V/msec to 1V/minute. The reference bias for IC_{1B} is 108 mV, which you derive from IC_{1D} as a unity-gain buffer for divider R_7 and R_8. R_6 ensures that you do not exceed IC_{1B}'s input current when you turn off the power, that C_1 discharges through IC_{1B}'s input and output diodes, and that IC_{1B}'s output does not excessively load back into IC_{1D}'s output with R_2 at a minimum.

R_3 and R_4 divide the saturated IC_{1A}'s output to approximately 100 mV unloaded above or below the 108-mV bias. This division causes approximately 20 mV to drop across R_5 to slew IC_{1B} upward or downward at the integration rate that C_1 and R_2 set; 20 mV is comfortably above the op amp's possible 3-mV input-offset voltage to minimize offset effects. When IC_{1B}'s output-voltage ramp reaches that of the input voltage from the R_1 wiper, IC_{1A} comes out of saturation and rests at approximately 2.5V, providing the loop-negative feedback to maintain integrator IC_{1B}'s output equal to the input voltage. This action sets the boundary on the integration ramp's terminal voltage. IC_{1C} can be spare, or, as the **figure** shows, you can drive it with a triangle-wave signal to convert IC_{1B}'s dc level or ramp to a corresponding PWM (pulse-width-modulated) signal for a motor-drive circuit (not shown).

R_5 eliminates differential errors arising from bias-resistor tolerance, and it provides a compromise between IC_{1B}'s 3V maximum input-offset voltage at 25°C and 20-mV input amplitude to allow the slowest dV/dt. The values in the **figure** result in a maximum time of approximately 1V/minute, or 5 minutes at V_{CC} of 5V to reach full speed. If you require longer times,

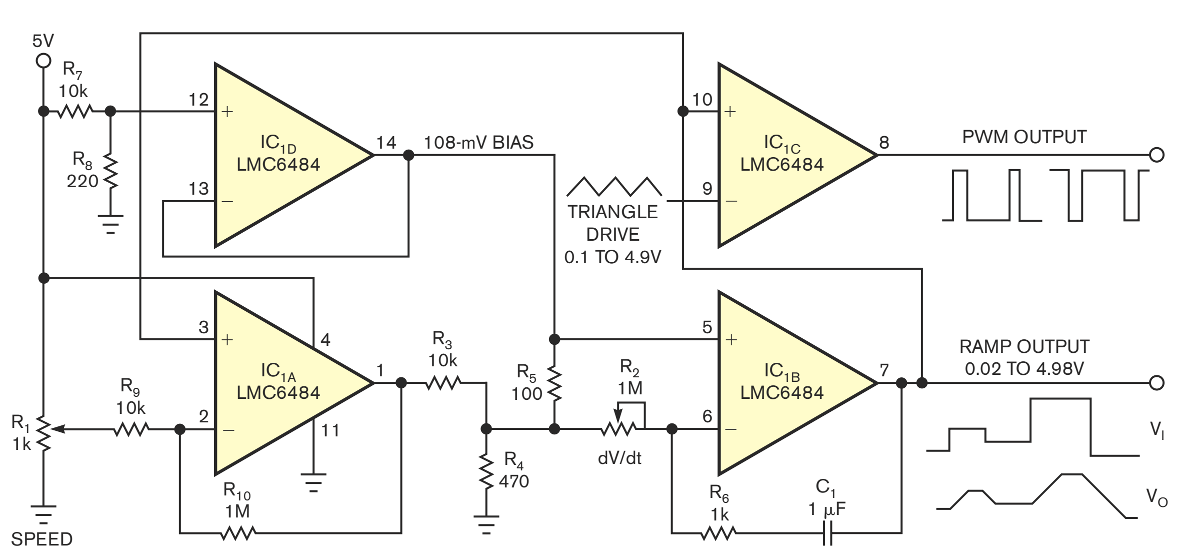

Figure 1 This op-amp integrator ramps up or down at a preset rate, holding a final value equal to the input-voltage dc level.

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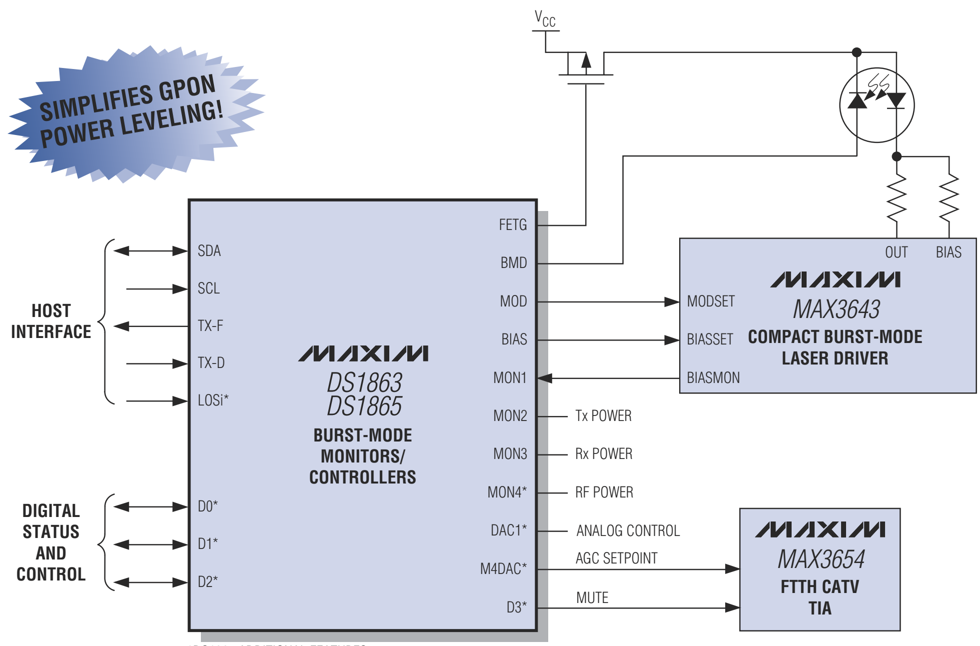

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you can raise V_{CC} to 15V with adjustments to the bias resistors or raise C_1's value by using parallel nonpolarized capacitors. Alternatively, you could raise R_2's value, although selection is sparser for potentiometers with values greater than 1 MΩ.

If your application does not require a long time constant or if you use the aforementioned methods to increase the time constant, you can eliminate R_5 at the expense of a higher level differential input to IC_{1B} and correspondingly faster integration. You could also eliminate IC_{1D} and the R_7-R_8 resistive-bias divider that connects directly to IC_{1B}'s Pin 5, but resistor tolerance becomes more critical to minimize differential error (**references 1** and **2**).EDN

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Switcher adds programmable-PWM-duty-cycle clamp

Michael O'Loughlin, Texas Instruments, Nashua, NH

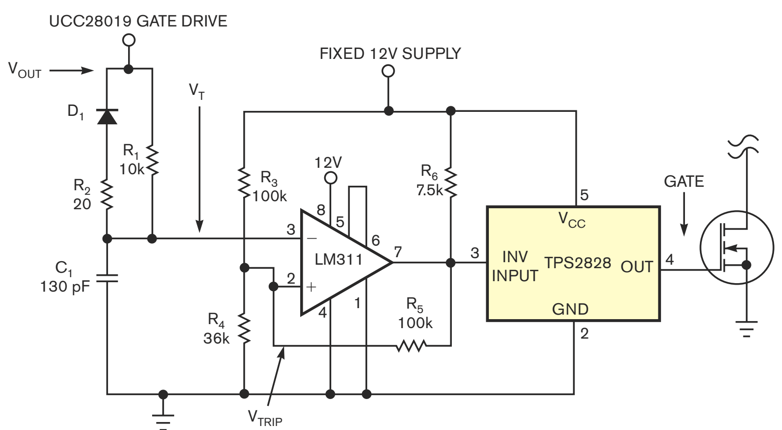

Figure 1 This simple circuit clamps the duty cycle of a switching regulator to 90%.

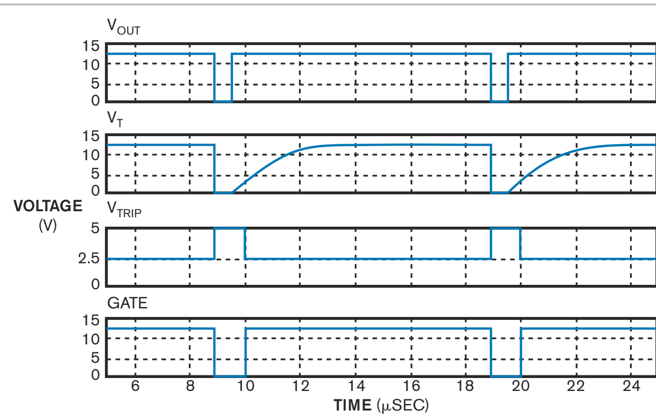

Figure 2 A SPICE simulation of the circuit in Figure 1 shows the clamping action cutting in at 90% duty cycle.

Power-supply applications require the use of a duty-cycle clamp. Such applications include those using current-sense transformers and two-switch forward converters. If a duty-cycle clamp is not present, the transformers could saturate, causing a catastrophic failure in the system. However, to drive down the cost of the design, many power-supply designers use inexpensive, eight-pin PWM controllers that have no duty-cycle clamp. This Design Idea shows how to add an inexpensive duty-cycle clamp to these PWM controllers.

You can add the circuitry to most PWM controllers to provide a programmable duty-cycle clamp (**Figure 1**). The circuitry comprises a few passive components, a hysteretic comparator, and a gate-driver IC. Resistor R_1 and capacitor C_1 program the duty-cycle clamp's dead time. Resistor R_2 and diode D_1 reset the timing circuitry when the output of the PWM controller goes low. Resistors R_3, R_4, and R_5 set the comparator's trip point, V_{TRIP}, at 5V. Resistor R_5 adds −2.5V of hysteresis to the comparator to ensure circuit stability.

The following example shows how to set the circuitry in **Figure 1** for a maximum duty cycle, D_{MAX}, of 0.9. The PWM controller operates at a switching frequency, f_S, of 100 kHz. Most PWM controllers cannot reach 100% duty cycle and have a specified dead time. For this example, the dead time is 300 nsec. To set the timing capacitor also requires knowing the maximum output of the PWM output voltage, V_{OUT}. In this example, the maximum output voltage is 12V. The timing ca-

pacitor is roughly 130 pF. The design uses a standard, 120-pF capacitor. The following **equations** describe the calculations: $t=(1-D_{MAX})(1/f_S)-$dead time=700 nsec, and

$$C_1 = \frac{-t}{\ln\left(1-\frac{V_{TRIP}}{V_{OUT}}\right)R_1} \approx 130\ \text{pF}.$$

A SPICE simulation with the circuitry in **Figure 1** ran to ensure that the duty-cycle clamp works with the circuitry. **Figure 2** shows the results of this simulation. V_{OUT} is the output of the PWM controller, V_T is the voltage at the inverting pin of the comparator, V_{TRIP} is the voltage at the noninverting input of the comparator, and gate is the output of the gate-driver IC. From the waveforms in **Figure 2**, you can see that the duty-cycle clamp appears to be working correctly, clamping the output of the gate driver to 90%.**EDN**

Circuit provides low-cost QAM mapping and translation

Pieter Demuytere, Cedric Mélange, Elena Matei, Els De Backer, Johan Bauwelinck, and Jan Vandewege, Ghent University, Department of Information Technology, Ghent, Belgium

This Design Idea presents an efficient way to do QAM (quadrature-amplitude-modulation) mapping and translation into two's-complement values with only two inverters and no look-up tables.

Suppose you want to create a 256-level QAM signal using a microcontroller and two 10-bit DACs with a parallel input in two's-complement notation. Because you can split a 256-level QAM signal into a 16-level ASK (amplitude-shift-keying) signal for the in-phase component and a 16-level ASK for the quadrature component, a symmetrical approach is feasible. The fully symmetrically circuit performs the 16-level ASK mappings and translations (**Figure 1**). Two inverters are the only glue logic you need for the conversion. Each part of the circuit converts four output bits of the microcontroller into a 10-bit two's-complement vector, which feeds directly to the DACs (**Table 1**). The possible DAC-input values are equally distributed. The third column of **Table 1** gives the normalized DAC output after an optional current-to-voltage conversion.

For 256-level QAM signals, you need 8 input bits, which exactly fit the width of a general-purpose-I/O bank on most microcontrollers. Simultaneously setting all 8 bits ensures synchronization between in-phase and quadrature signals. You can easily adapt this circuit for any QAM constellation or DAC resolution. Because this circuit is fully digital, you can also embed it in FPGAs or CPLDs, using the inverters available in the output buffers.**EDN**

TABLE 1 INPUT AND OUTPUT

Microcontroller output	DAC input	DAC output (V)
0000	1000 0000 10	–0.998
0001	1001 0001 10	–0.863
0010	1010 0010 10	–0.730
...	...	...
0111	1111 0111 10	–0.066
1000	0000 1000 10	0.066
...	...	...
1101	0101 1101 10	0.730
1110	0110 1110 10	0.863
1111	0111 1111 10	0.998

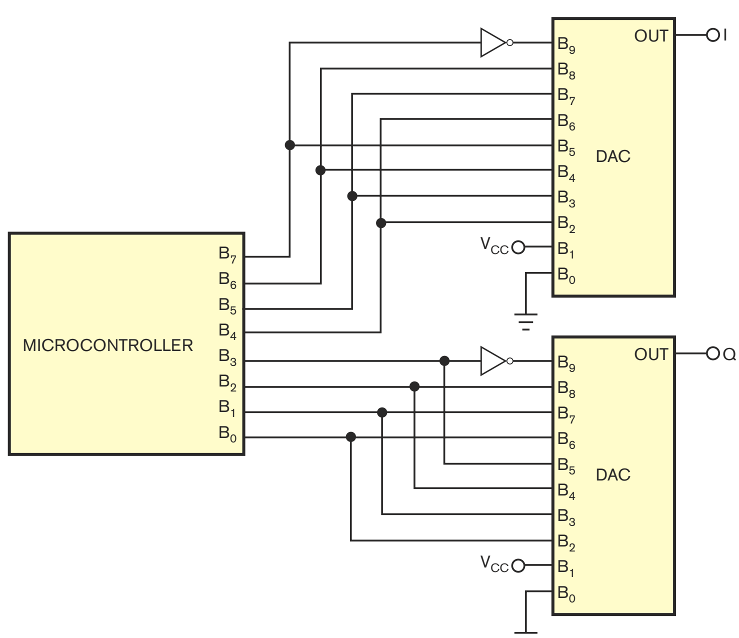

Figure 1 This circuit converts 2×4-bit outputs from the microcontroller into 2×12-bit, 16-level ASK values.


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DESIGN NOTES

High Power PoE PD Interface with Integrated Flyback Controller

Design Note 425

Dilian Reyes

Introduction

To this day, Power over Ethernet (PoE) continues to gain popularity in today's networking world. The 12.95W delivered to the Powered Device (PD) input supplied by the Power Sourcing Equipment (PSE) is a universal supply. Each PD provides its own DC/DC conversion from a nominal 48V supply, thus eliminating the need for a correct voltage wall adapter. However, higher power devices can not take advantage of standard PoE because of its power limitations, and must rely on a large wall adapter as their primary supply. The new LTC4268-1 breaks this power barrier by allowing for power of up to 35W for such power-hungry 2-pair PoE applications. The LTC4268-1 provides a complete solution by integrating a high power PD interface control with an isolated flyback controller.

PD Interface Controller

The PD interface controller provides the same 25k signature detection resistance defined in the standard PoE. An extended optional class can be read by a customized PSE that looks for such a class. Once a PSE detects and classifies the PD, it fully powers on the device. The LTC4268-1 provides a low inrush current limit, allowing load capacitance to ramp up to the line voltage in a controlled manner without interference from the PSE current limit. After the load capacitance is charged up, the LTC4268-1 switches to the high input current limit and provides a power good signal to its switching regulator indicating that it can start its operation. During this time, the LTC4268-1 remains in its high current limit state allowing for up to 35W delivered to the load.

Synchronous Flyback Controller

Once power is switched over to the synchronous flyback controller, the LTC4268-1 regulates the output voltages by sensing the average of all the output voltages via a transformer winding during the flyback time. This allows for tight output regulation without the use of an

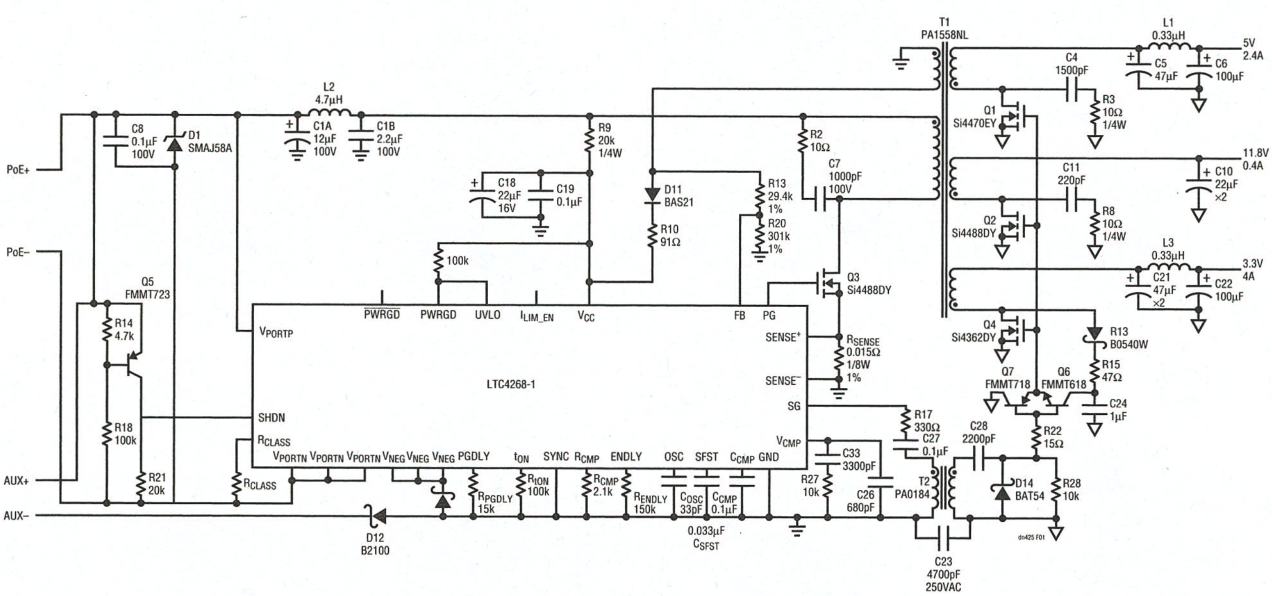

Figure 1. High Efficiency, Triple Output, High Power PD

optoisolator, providing improved dynamic response and reliability. Synchronous rectification increases the conversion efficiency and cross-regulation effectiveness above a conventional flyback topology. No external driver ICs or delay circuits are needed to achieve synchronous rectification; a single resistor is all that is needed to program the synchronous rectifier's timing.

High Efficiency, Triple Output, High Power PD

Figure 1 shows a design using the LTC4268-1 in a high power, triple output PD. A high power PSE connects through an Ethernet cable to the RJ45 connector. PSE detection and power is passed through the data pairs' high power Ethernet transformer or directly to the spare pairs in this 2-pair 10/100BaseT PoE system. The PSE power is then controlled by the LTC4268-1 PD interface and forwarded on to its switching regulator. An auxiliary supply option can also be connected to bypass and disable the PD interface which gives the auxiliary priority in power supply over PoE. Power conversion is then from the auxiliary supply down to the output voltages.

The small supply of the LTC4268-1 utilizes an isolated flyback topology with synchronous rectification that requires no optoisolator, lowering the parts count. This circuit gives efficiencies at full load of 83% when powered from a PSE and over 85% power sourced from an auxiliary supply.

PSE and Auxiliary Supplies

Standard PSEs are capable of providing as low as 15.4W at the port output. This would not be sufficient power for a high power PD operating at full load. Here, a customized PSE capable of delivering higher power must be used, or a PSE controller designed for high power such as an LTC4263-1 single port PSE controller. In cases where a high power PSE is not available, an auxiliary supply can be used.

2-Pair vs 4-Pair PD

2-pair power is used today in IEEE 802.3af systems. One pair of conductors is used to deliver the current and a second pair is used for the return while two conductor pairs are not powered. This architecture offers the simplest implementation method but suffers from higher cable loss than an equivalent 4-pair system.

4-pair power delivers current to the PD via two conductor pairs in parallel allowing for an even higher level of power. This lowers the cable resistance but raises the issue of current balance between each conductor pair. Differences in resistance of the transformer, cable and connectors along with differences in diode bridge forward voltage in the PD can cause an imbalance in the currents flowing through each pair. Using two independent LTC4268-1s (Figure 2) allows for interfacing and power from two independent PSEs, and independent DC/DC converters resolve the current imbalance.

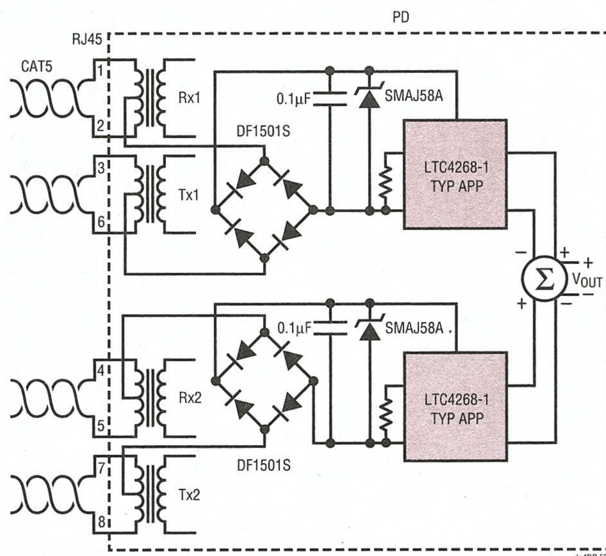

Figure 2. 4-Pair, High Power PD Diagram

Conclusion

The LTC4268-1 is a highly integrated solution for the next generation of PD products. It offers PoE PD functionality with control for efficient high power delivery to the output load.

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productroundup

AMPLIFIERS, OSCILLATORS, AND MIXERS

DC-TCXO provides high accuracy over a wide temperature range

The DS4026 DC-TCXO (digitally controlled temperature-compensated-crystal oscillator) features a ±1-ppm frequency accuracy and stability over −40 to +85°C. Over a 10-year operational life, the device provides a ±4.6-ppm accuracy and phase-noise performance with 140-dBc/Hz at a 1-kHz offset characteristic. Using a proprietary design and calibration techniques, the oscillator negates the effects of electromechanical stress, thermal variations, and frequency perturbations also known as activity dips. Using finite step-compensation methods, the device overcomes the noisy design typical of digital TCXOs. The oscillators are factory-calibrated to compensate their embedded crystal's natural temperature characteristics. Additional features include a 3°C accurate and readable temperature sensor and a 16-bit DSP-controlled DAC for frequency stability, trimming, and calibration. An I^2C control interface allows for frequency trimming and temperature reading. You can tune the frequency with a resolution better than 1 ppm. Operating from a 3.3V supply voltage, the device comes in a 300-mil ROHS (restriction-of-hazardous-substances)-compliant SO-16 package. The DS4026 DC-TCXO costs $20 (10,000).

Maxim Integrated Products, www.maxim-ic.com

Precision amplifier provides low noise for single-supply applications

Combining a 25-μA maximum offset voltage and a 5.5-MHz bandwidth, the OPA376 suits low-noise, precision amplifiers for filtering, data-acquisition, and single-supply-processing systems. Targeting sensor and signal conditioning, wireless communications, medical instrumentation, handheld test equipment, and consumer-audio equipment, the amplifier provides a 950-μA maximum quiescent current and a 7.5-nV/$\sqrt{Hz}$ noise density. Additional features include CMOS-process technology, less than 1-mA quiescent current, and 1-μV/°C maximum-temperature-drift characteristics. Available in SC70, SO-8, and SOT23-5 packages, the OPA376 costs 65 cents (1000).

Texas Instruments, www.ti.com

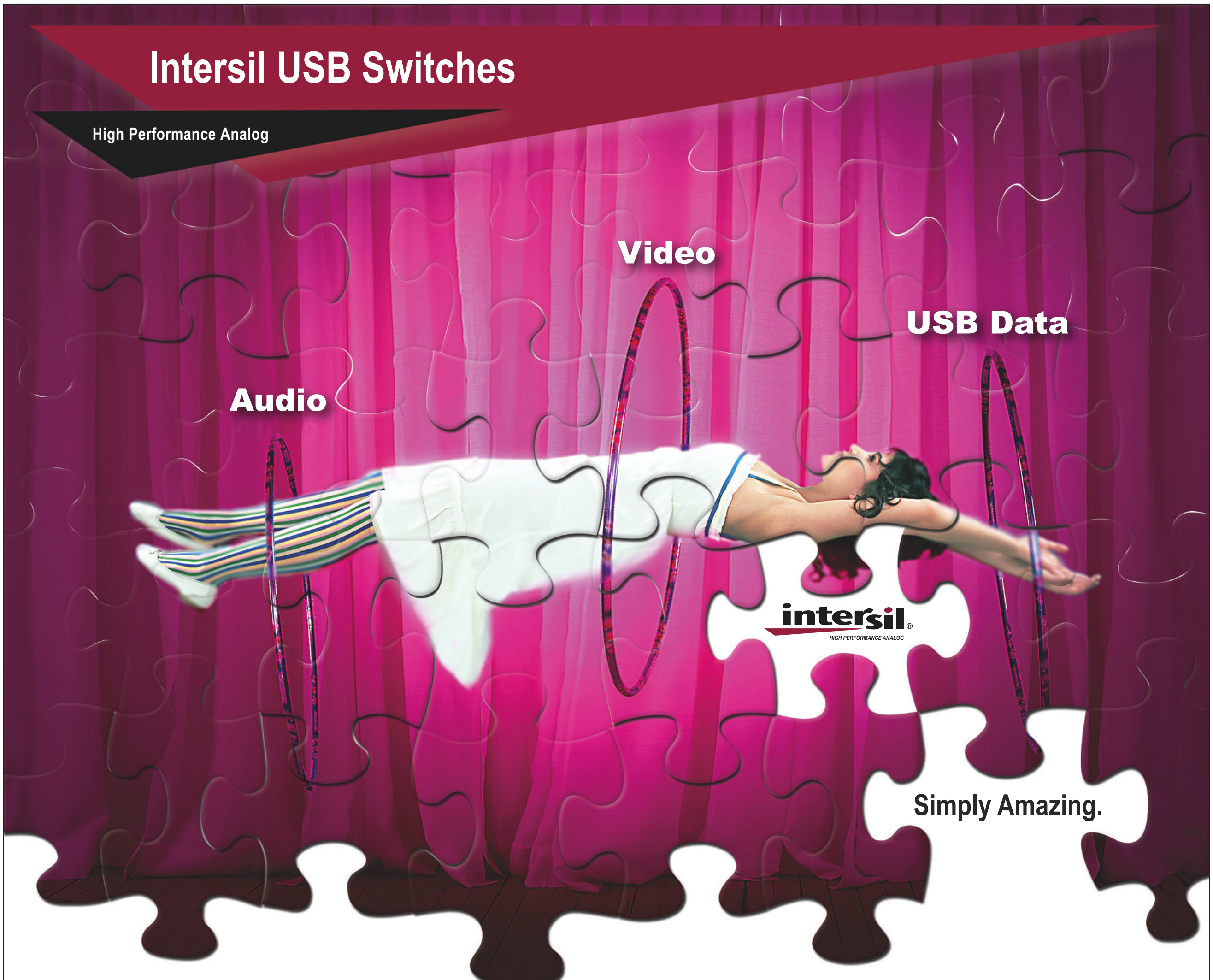
I/O op amp swings within 100 mV from the rails

Operating over a 2.7 to 5.5V power-supply range, the high-output-drive AS1710 rail-to-rail I/O operational amplifier swings within 100 mV from the rails and sinks or sources 50 mA of output current. Features include a 200-mA peak current, a 10-MHz unity-gain bandwidth, a 10V/μsec slew rate, and a 50-pA bias current. The amplifier requires a 1.6-mA supply current and 1 nA in shutdown mode. Available in a SC70-6 package, the AS1710 op amp costs 18 cents (1000).

Austriamicrosystems, www.austriamicrosystems.com

Programmable-gain amplifier features 0.03% gain accuracy

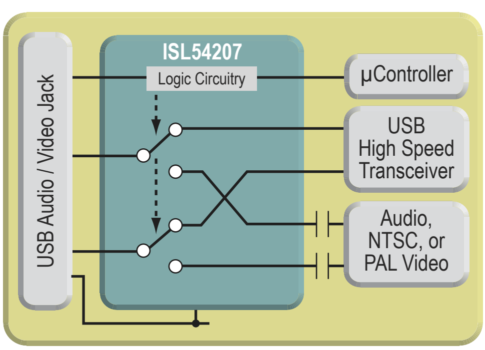
Delivering 0.03% gain accuracy, the LMP8100A precision programmable-gain amplifier uses a software-adjustable gain in 1V/V increments from 1 to 16V/V over the −40 to +125°C industrial-temperature range. An array of 16 precision thin-film resistors sets the amplifier's closed-loop gain. At the core of the device, a precision 33-MHz CMOS-input, rail-to-rail-I/O operation amplifier provides a 110-dB typical open-loop gain. Providing four levels of internal frequency compensation, the higher gain settings increase the usable signal bandwidth. The input-zero-calibration feature allows users to measure the output offset voltage to calibrate any errors resulting from temperature or voltage shifts. Users program control modes with a serial port, allowing cascading of several devices. Additional features in-

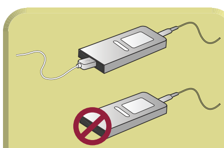


Intersil's tiny USB Switch **enables charging, audio, video, and high speed data through a single connector.**

Audio / Video / Data

Device	Audio THD 32Ω (%)	USB Speed	Video Diff Gain Phase
ISL54207	0.06	480	0.28 / 0.04
ISL54208	0.06	480	0.28 / 0.04
ISL54415	0.007	12	0.04 / 0.03
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03





Combined data, audio, and video switch eliminates either the USB or TV OUT connector on cameras or media players.

Audio / Data

Device	Audio THD 32Ω (%)	USB Speed
ISL54205A	0.06	480
ISL54206	0.06	480
ISL54400	0.007	12
ISL54401	0.007	12
ISL54402	0.007	12

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AMPLIFIERS, OSCILLATORS, AND MIXERS

clude a 12V/μsec slew rate, 33-MHz unity-gain bandwidth, 2.7 to 5.5V supply-voltage range, 5.3-mA supply current, 20-mA output current, and 20-μA power consumption in shutdown mode. The amplifier also uses the vendor's VIP50 BiCMOS-process technology. Available in an SOIC-14 package, the LMP8100A amplifier costs $7 (1000).
National Semiconductor, **www.national.com**

Precision 16V op amps come in single- and dual-channel versions

Targeting battery-operated applications, the 16V precision AD8663 rail-to-rail operational amplifier suits patient monitors, defibrillators, remote industrial controls, and optical sensors. Manufactured using the vendor's iCMOS high-voltage industrial process, the device also incorporates the vendor's DigiTrim in-circuit-trimming technology. This technology provides a low offset voltage, a 90-dB CMRR (common-mode-rejection ratio), and a 105-dB PSRR (power-supply-rejection ratio). Operating over a 5 to 16V operating range, the device consumes 180 μA. The AD8667 dual-channel version is also available. The AD8663 comes in an LFCSP-8 or SOIC-8 package and costs 64 cents and 80 cents (1000), respectively. The AD8667 comes in MSOP-8 and SOIC-8 housing and costs 80 cents and 78 cents (1000), respectively.
Analog Devices, **www.analog.com**

COMPUTERS AND PERIPHERALS

Quad-core processor operates at 2.93 GHz

Using the vendor's Core microarchitecture for quad-core desktops, the QX6800 Core 2 Extreme Quad processor operates at 2.93 GHz. The vendor's 65-nm process enables an 8-Mbyte cache. Supporting a 1066-MHz system bus, the QX6800 costs $1199.
Intel, **www.intel.com**

Hard-drive kit includes built-in eSATA/SATA

Featuring a built-in eSATA/SATA, the Diamond hard-drive kit provides removable SATA-drive-cartridge storage. A high-performance eSATA port allows the device to attach externally to any computer, or users can employ the device as a drive cartridge in the hard drive's cradle, inside a 5.25-in. drive bay. A computer using eSATA or USB connection can access the device using the vendor's eSATA adapter. A user can install any 2.5-in. SATA hard drive in the drive enclosure using an optional hard-drive-mounting bracket. The Diamond Combo hard drive includes a Diamond hard-drive enclosure, a Diamond SATA drive cradle with a SATA interface, a six-foot eSATA data cable, and a 110/220V ac/dc 12V/5V power adapter for using the drive enclosure as an external hard drive. The Diamond Combo hard drive costs $49.95.
Addonics Technologies, **www.addonics.com**

Wide-format displays feature a 1000-to-1 contrast ratio

Joining the vendor's AccuSync Series, the 19-in. ASLCD193WXM, 20-in. ASLCD203WXM, and 22-in. ASLCD223WXM wide-format displays feature integrated speakers, a

productroundup

COMPUTERS AND PERIPHERALS

5-msec response time, and a 1000-to-1 contrast ratio. The ASLCD193WXM has a 1440×900-pixel native resolution, and the ASLCD203WXM and ASLCD-223WXM provide a 1680×1050-pixel native resolution. The ASLCD193-WXM, the ASLCD203WXM, and the ASLCD223WXM cost $229.99, $289.99, and $359.99, respectively.

NEC Display Solutions of America, www.necdisplay.com

18× DVD±R burner has SATA support

Featuring SATA support, the internal TurboPlex PX-810SA DVD Super multidrive provides 18× DVD±R on single-layer media, 10× DVD±R on double- and dual-layer media, and 12× DVD-RAM. The DVD-±VR supports direct-disc recording, and the DVD±RW background format eliminates the need to manually format a DVD±RW disc. Additional support includes 8× DVD±R, 6× DVD-RW, 16× maximum DVD-ROM, 40× CD-R/ROM, 32× CD-RW, and 12× DVD-RAM. Compatible with the Windows Vista operating system, the drive features a 2-Mbyte buffer and Buffer Underrun Proof Technology, which prevents buffer-underrun errors and allows multitasking. The TurboPlex PX-810SA costs $89.

Plextor LLC, www.plextor.com

EDA TOOLS

EM simulation tool verifies hearing-aid compatibility

Aiming at modeling and verifying antennas and antenna systems, the second release of the vendor's AMDS (Antenna-Modeling-Design System) EM (electromagnetic)-simulation tool contains capabilities verifying that handheld wireless devices are compatible with hearing aids. Version 2007.4 allows users to evaluate hearing-aid compatibility between wireless-communication devices and hearing aids, according to the IEEE American National Standard Methods of Measurement of Compatibility, ANSI C63.19-2006. This standard establishes categories of compatible hearing aids and wireless devices. The 3-D EM set includes efficient importation of CAD data from production designers, reducing or eliminating EM-design iteration, as well as verification of antenna compliance with legal and operational standards such as over-the-air performance and MIMO (multiple input/multiple output). The simulator also features optimization of MIMO performance by analyzing antenna placement and diversity for the entire physical wireless appliance and simulating the device's real-world interaction with the human body to improve performance. The tool costs $50,000.

Agilent Technologies, www.agilent.com

Free simulation kit for PCBs uses Actel's Arria FPGAs

The CR-5000 simulation-design kit assists with the integration of Altera's Arria GX FPGAs onto PCBs (printed-circuit boards). The set of topology templates makes routing to JEDEC-defined signaling standards, including SSTL 1.8V, a straightforward process. Using waveform and eye-pattern analysis in addition to simulation models, the kit allows comparing of real-board performance with the theoretical ideal. Assisting in electromagnetic compatibility, the kit allows users to view results in the time and frequency domains, displaying voltage and current. Users import the design kits from the vendor's support LinkZ Web site at no cost with a LinkZ login.

Zuken, www.zuken.com

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LOOKING AHEAD

TO THE POWER ELECTRONICS TECHNOLOGY CONFERENCE

Opening Oct 30 and running through Nov 1 in Dallas, the Power Electronics Technology Exhibition and Conference has retuned, its sponsors say, to focus on the greatest innovations in power design. The keynote and general-session address highlight two of these innovations. One session covers opportunities to improve efficiency in power electronics, and the other covers the ROHS (restriction-of-hazardous-substances) situation in China. Tutorials cover subjects ranging from basics of components to motor control and energy harvesting. Technical tracks include power design; applications, including the use of ZigBee for energy management; and components.

LOOKING AROUND

AT THE RISE OF THE ROBOTS

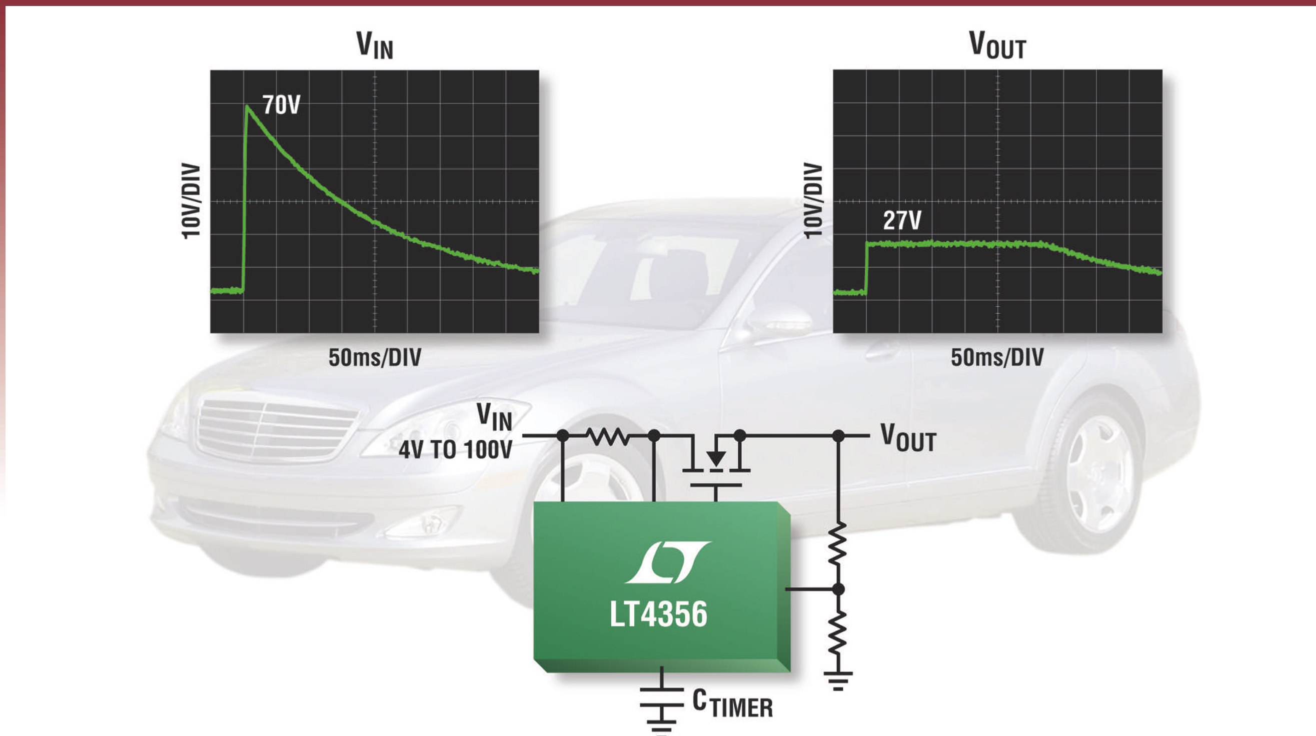
Technical Editor Paul Rako points out an interesting conference coming up next month in San Jose, CA: Robo Development 2007, billed as the first industry event for design and development of robots targeting use outside the laboratory environment and for sale at a profit. This definition implicitly includes that the robots in question are primarily mobile and autonomous—not simply advanced numerically controlled tools. Sometimes, the arrival of a conference signals the presence of enough activity in an area for infrastructure and professional communications to be important and that products are on the way. Plastic dogs and vacuum cleaners move over: These folks could be about to unseat all our assumptions about the feasibility, cost, and ubiquity of robots that can be assistants and associates, not just appliances.

LOOKING BACK

AS ASYNCHRONOUS DESIGN COMES TO SUPERCOMPUTING

The Maniac II computer uses a fast memory unit, any of whose 12,288 48-bit words can be located, brought out, and put back in about 8 μsec. The unit stores information on the faces of 98 3-in. cathode-ray tubes. Three subsidiary magnetic-tape memories can read or write at 600 words/sec. The Los Alamos computer does not have an internal clock but performs successive operations as rapidly as possible without pausing for a given number of clock cycles. Typical operating times are: for addition and subtraction, 18 μsec and, for multiplication, 170 μsec. —*Electrical Design News*, September 1957

Surge Stopper



Regulate Overvoltages & Overcurrents

Electronic systems prone to overvoltage and overcurrent events require sound front-end protection to ride out surges and maintain reliable operation in high availability systems. The LT®4356 replaces complicated protection circuitry with a simple IC/FET solution. During an overvoltage event, the LT4356 regulates the output to a user-defined voltage, while a fault timer ensures safe shutdown of the MOSFET if the fault persists. The LT4356 offers complete protection with inrush limiting, overcurrent and reverse input protection.

Features

- Wide Operating Range: 4V to 100V
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- Reverse Input Protection to -30V
- Adjustable Fault Timer
- Overcurrent Protection
- Inrush Current Limiting
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